

Topstar Digital technologies Co.,LTD

Board name: Mother Board Schematic
Project name: N01
Version: VerA
initial Date:
New update:

- 1. System Block Diagram & Schematic page description;
- 2. Power Block Diagram & Discription;
- 3. Annotations & information;
- 4. Schematic modify Item and history;
- 5. Power on & off Sequence;
- 6. ACPI Mode Switch Timings;
- 7. Power On Sequence Map;
- 8. CLOCK Distribution;
- 9. Power Distribution;

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Hardware drawing by:

Hardware check by:

EMI Check by:

Power drawing by:

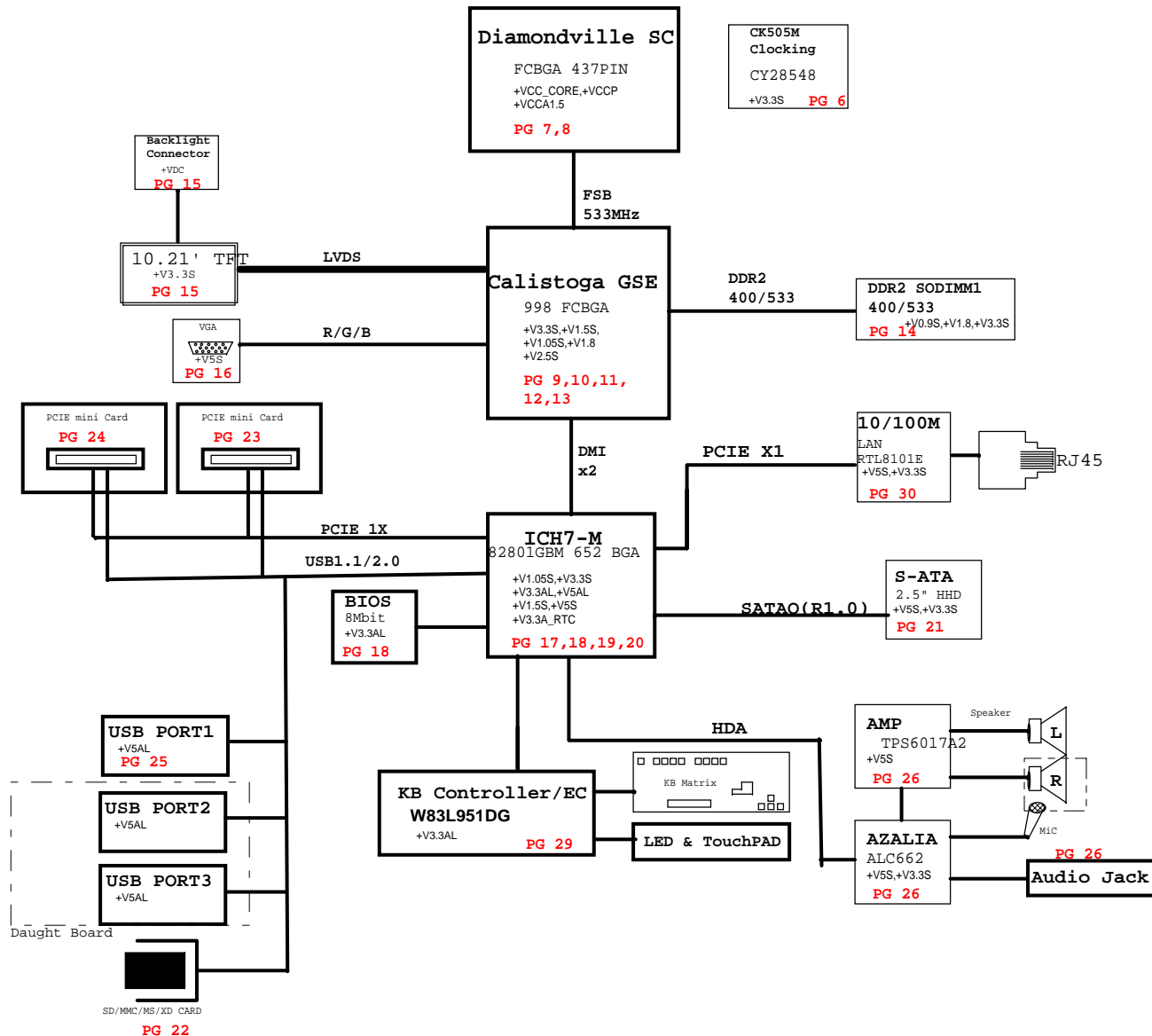
Power check by:

Manager Sign by:

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ShenZhen Topstar Industry Co.,LTD

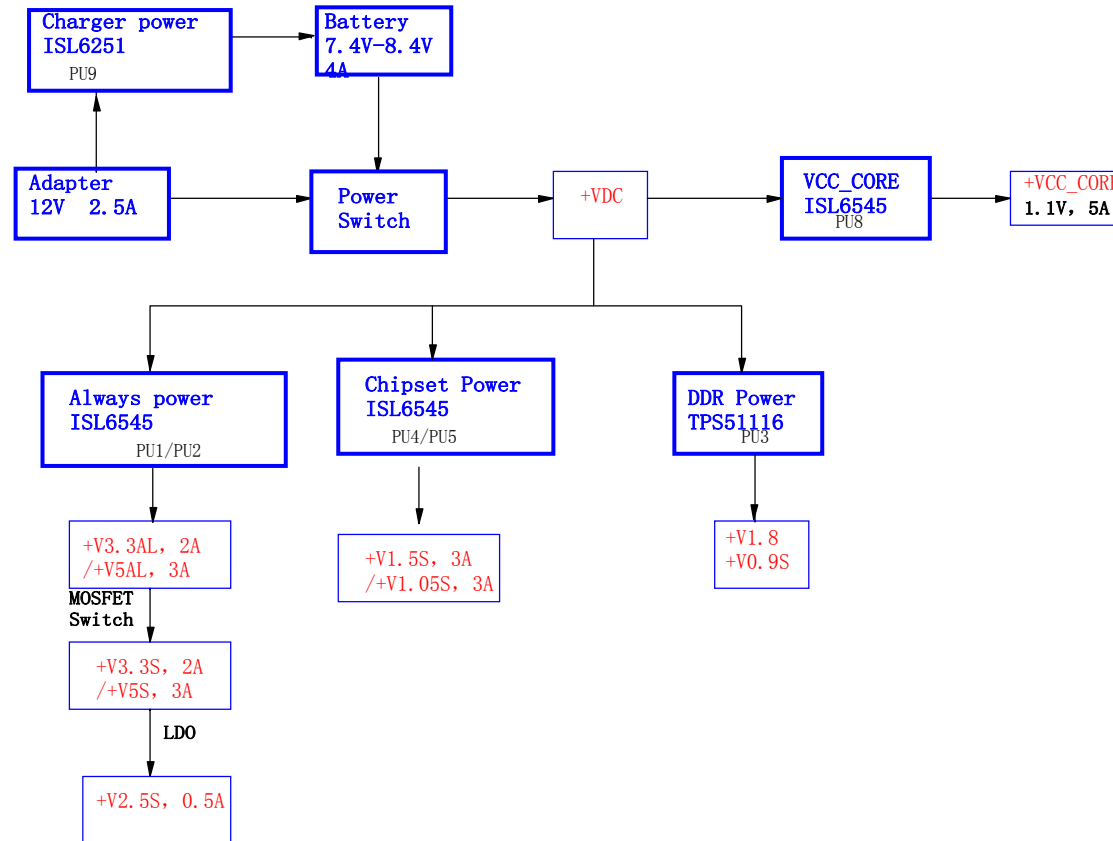
N01 SYSTEM BLOCK Ver:A



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N01 POWER BLOCK Ver:A



Voltage Rails

+VDC	Primary DC system power supply (6V-9.5V)
+VBATTERY	Battery Power supply (6-8.4V)
+VCC_CORE	Core Voltage for CPU
+V1.05S	1.05V for Calistoga & ICH7M core / FSB VTT
+V1.8	1.8V power rail for DDR2
+V0.9S	0.9V DDR2 Termination voltage
+V3.3AL	3.3V always on power rail
+V5AL	5V for ICH7-M's VCC5 Refsus
+V3.3S	3.3V main power rail
+V5S	5V main power rail
+V2.5S	2.5V power rail for 945GMS

Board stack up description

PCB Layers	Trace Impedence:55ohm +/-15%
Top(Signal1)	
VCC 2	
Signal 3	
Signal4	
Ground 5	
Bottom(Signal6)	

USB Table

USB Port#	Function Description
0	Standard USB2.0 Port
1	Standard USB2.0 Port
2	Standard USB2.0 Port
3	MINICARD_USB
4	CAM_USB
5	MINICARD_USB
6	CR_USB
7	NC

I2C SMB Address

Device	Address	Hex	Master
Clock Generator	1101 001x	D2	ICH7-M
SO-DIMMO	1010 000x	A0	ICH7-M
CPU Thermal Sensor	1001 100x	98	KBC
Smart Battery	0001 011x	16	KBC
PCIE Slot	TBD	TBD	ICH7-M

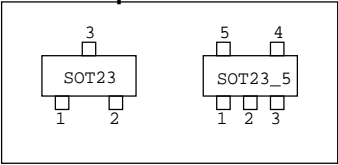
Power States

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clock
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(STM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(SoftOff)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Wake up Events


LID switch from EC
Power switch from EC

PCB Footprints



ns: Component marked "ns" is not stuff

Schematic modify Item and history:



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Page Name

Sch Modify and history

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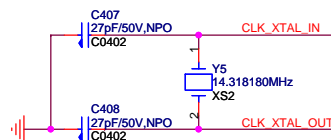
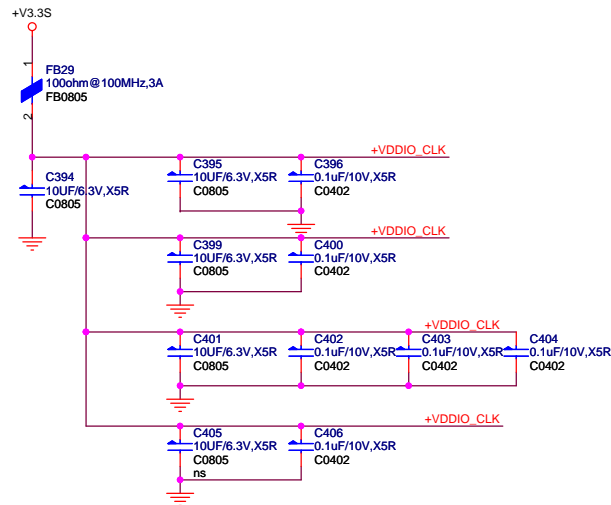
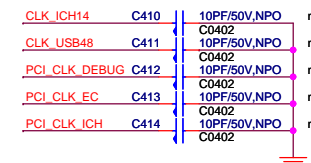
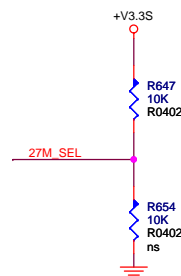
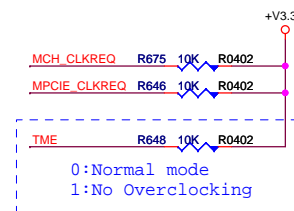
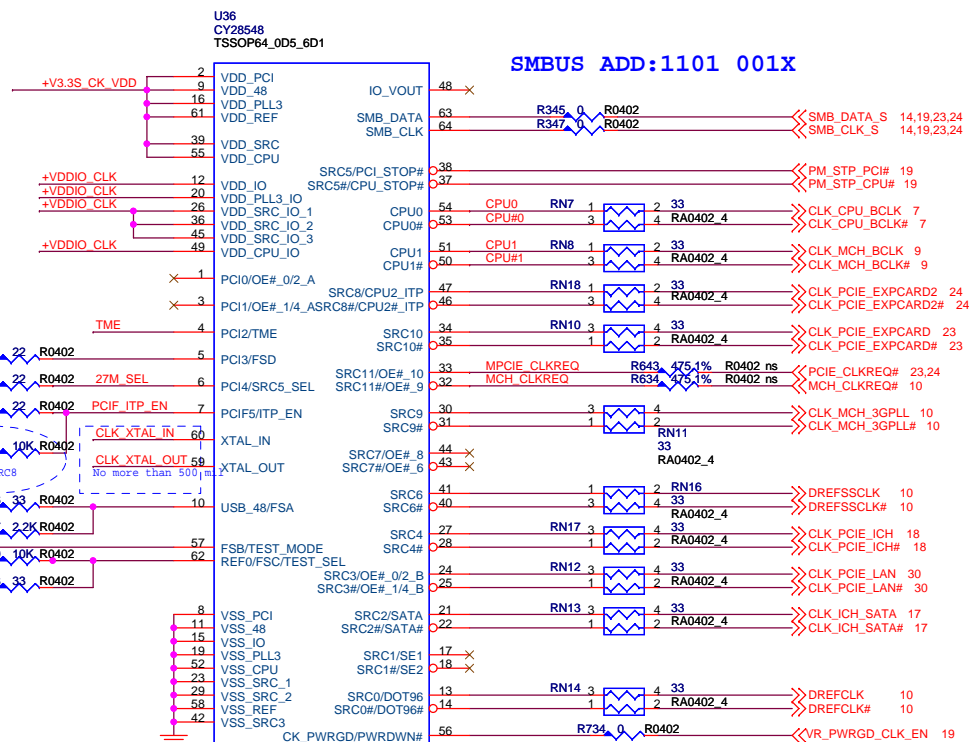
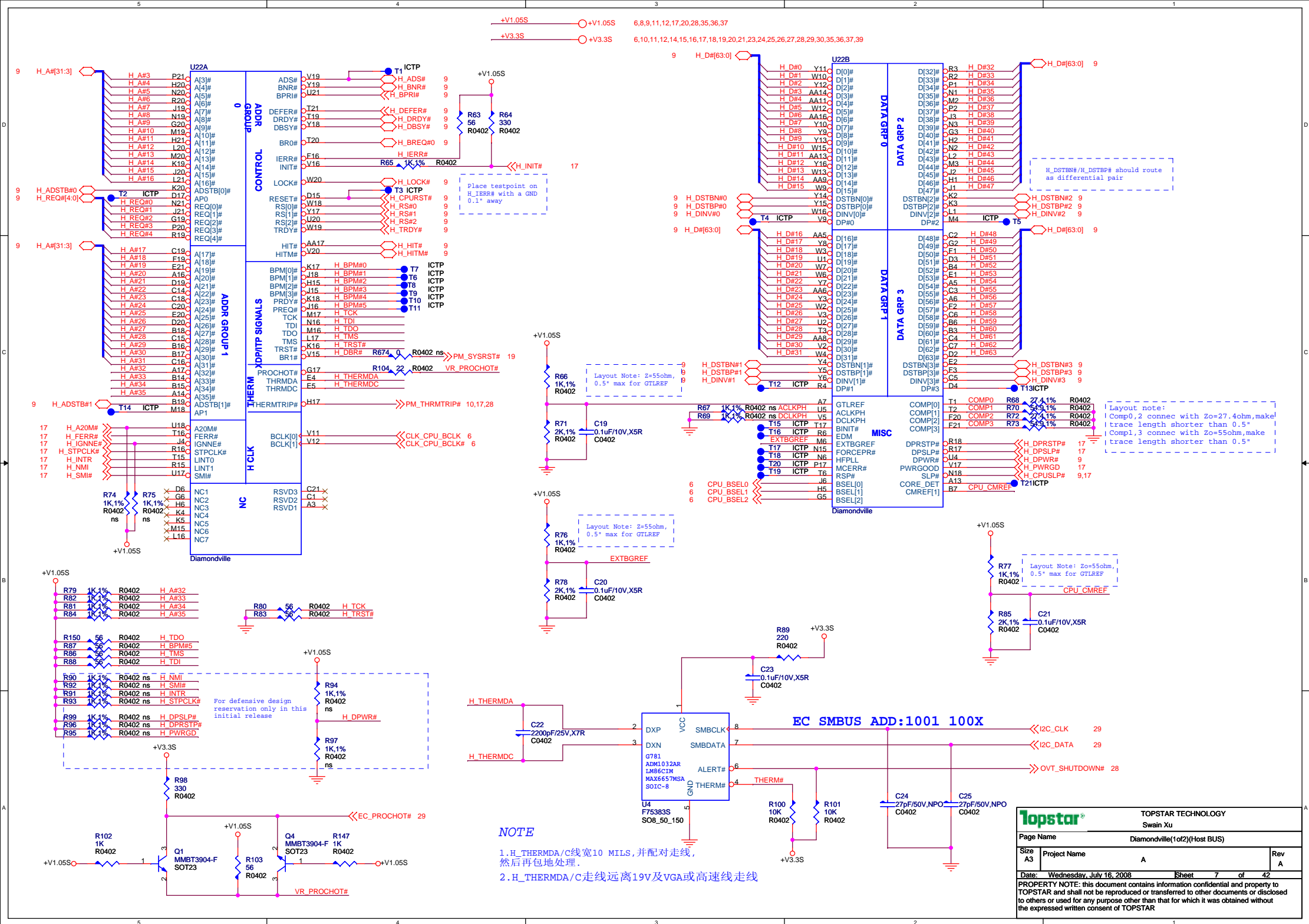


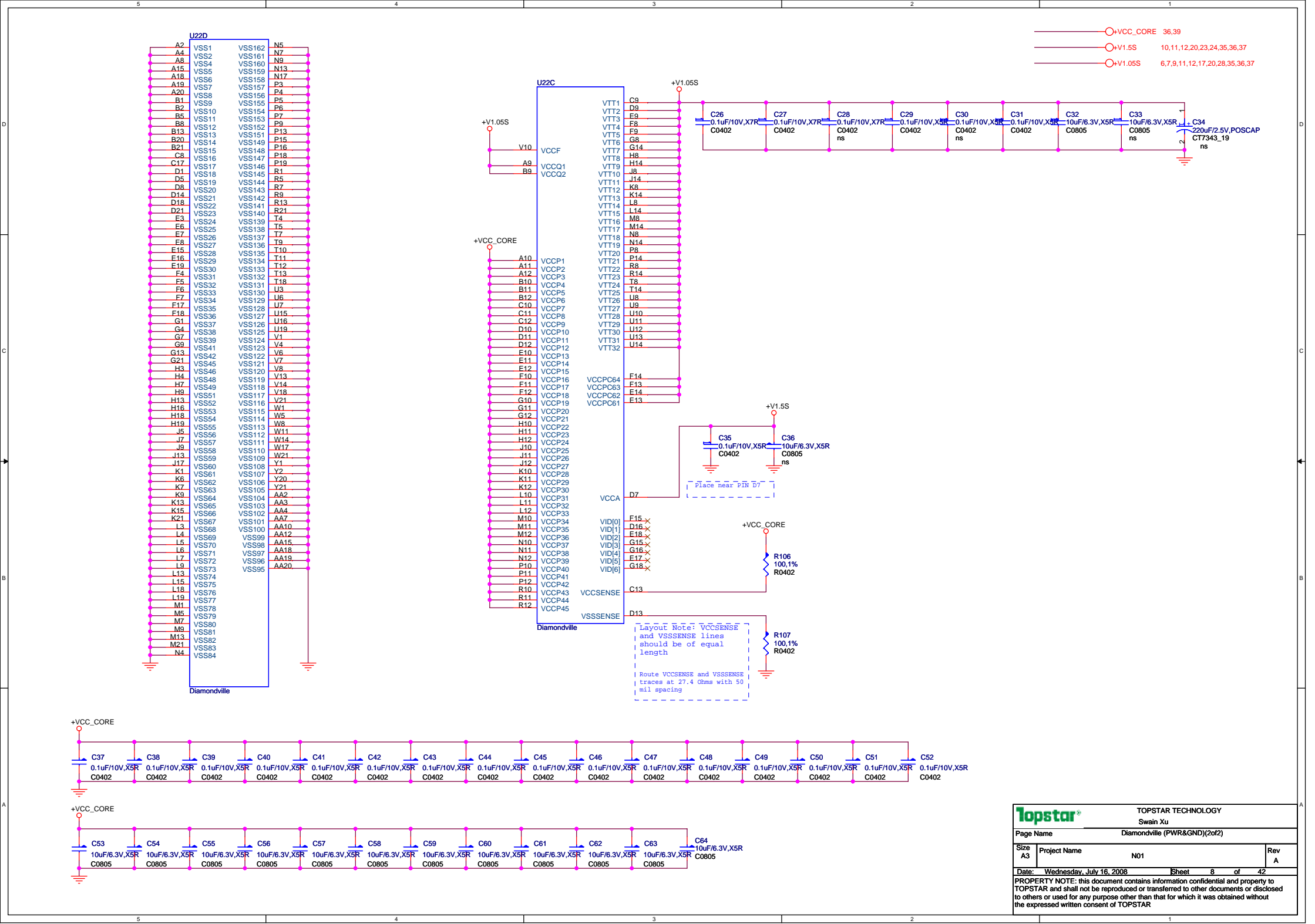
Diagram illustrating the CPU to MCH bus interface. The CPU signals (CPU_BSEL0, CPU_BSEL1, CPU_BSEL2) are connected to the MCH signals (MCH_BSEL0, MCH_BSEL1, MCH_BSEL2) via a series of resistors (R642, R651, R652) and 0 ohm jumpers (R0402). The power supply +V1_05S is connected to the top of the resistors. A capacitor C409 (0.1uF/25V,Y5V) is connected to the top of the resistors and ground.

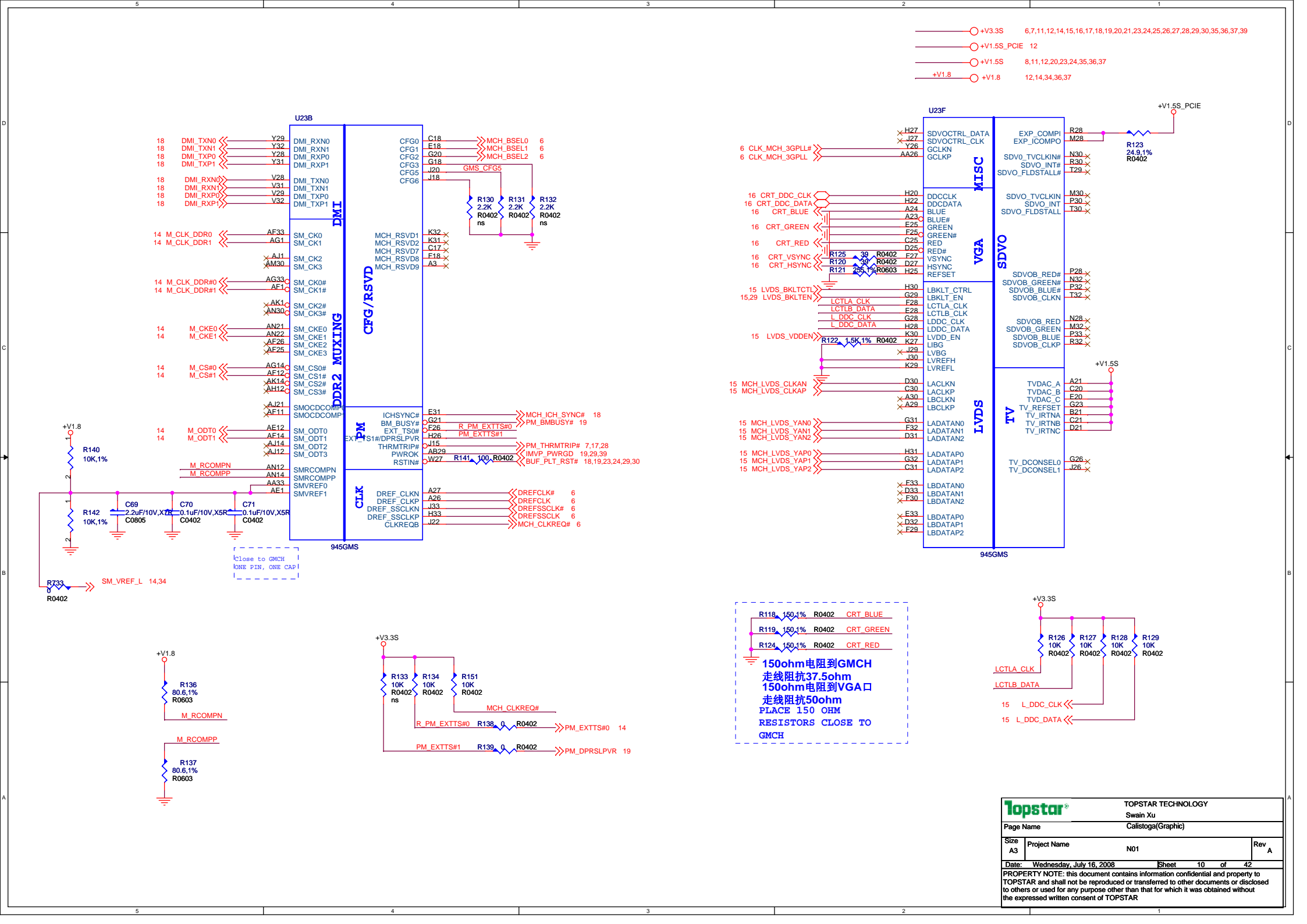
FSC	FSB	FSA	HOS
BSEL2	BSEL1	BSEL0	fr
0	0	1	1

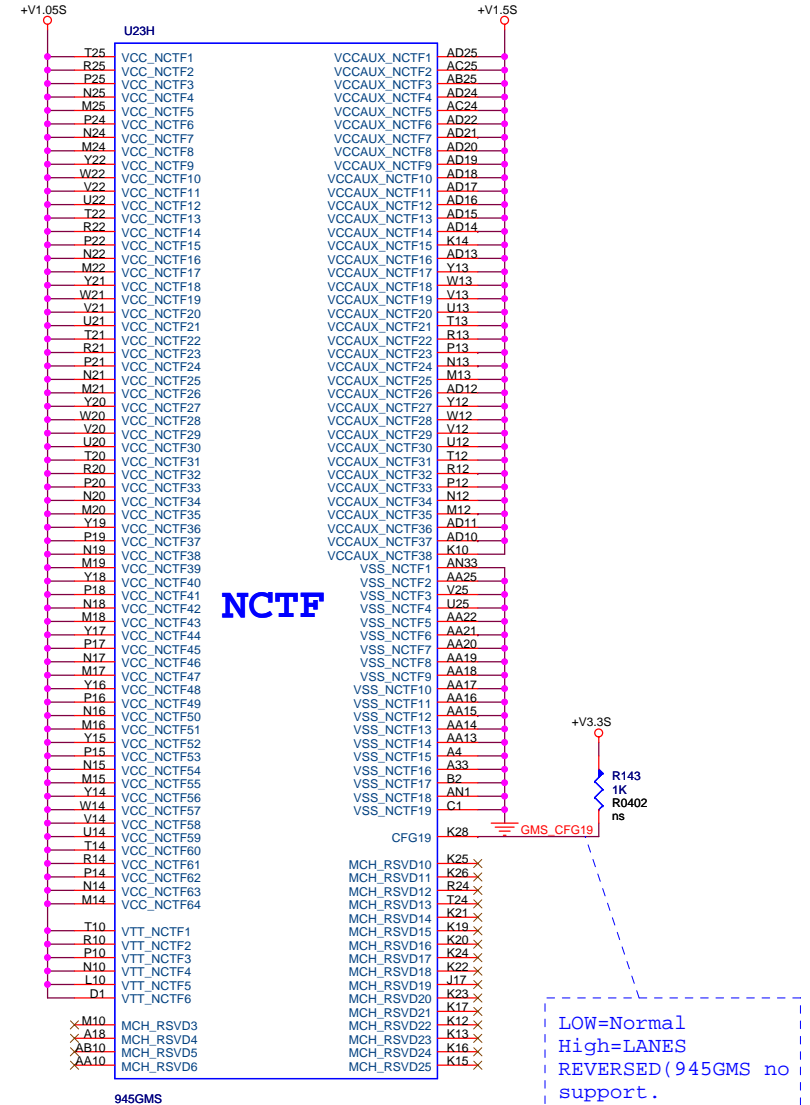
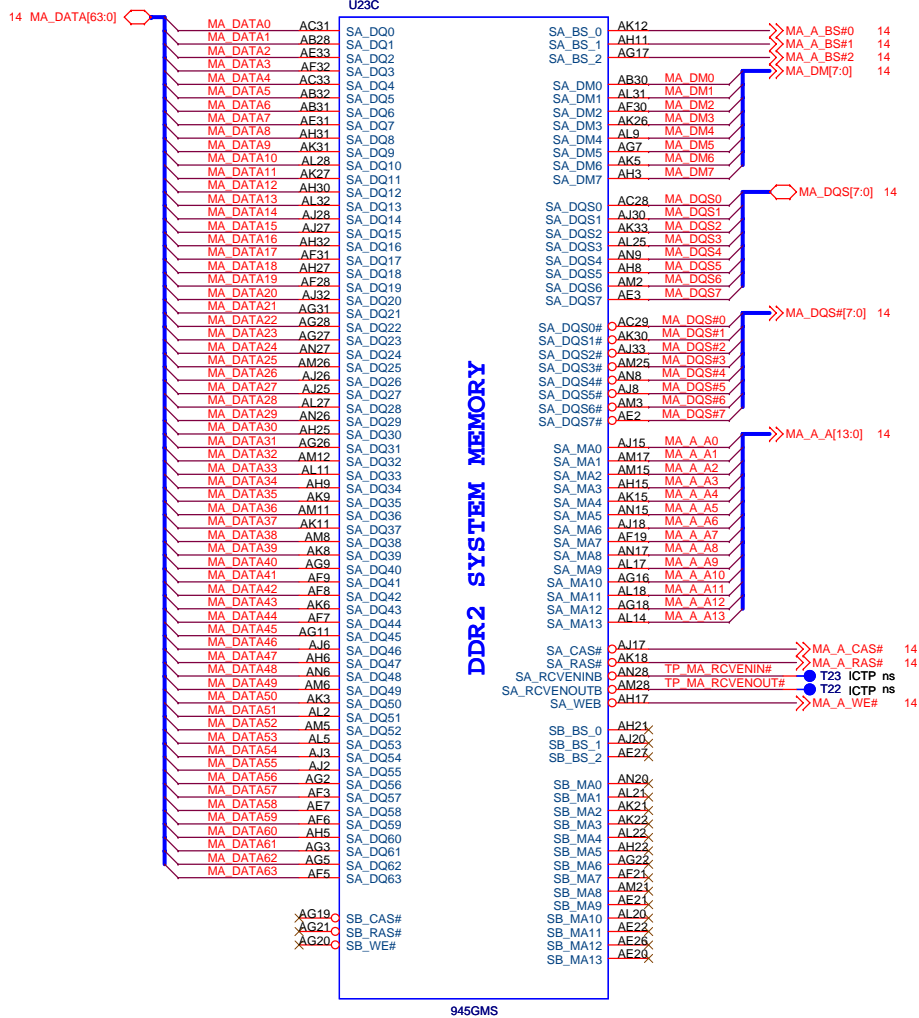
FSC BSEL2	FSB BSEL1	FSA BSEL0	HOST Clock frequency
0	0	1	133MHz
1	0	1	100MHz

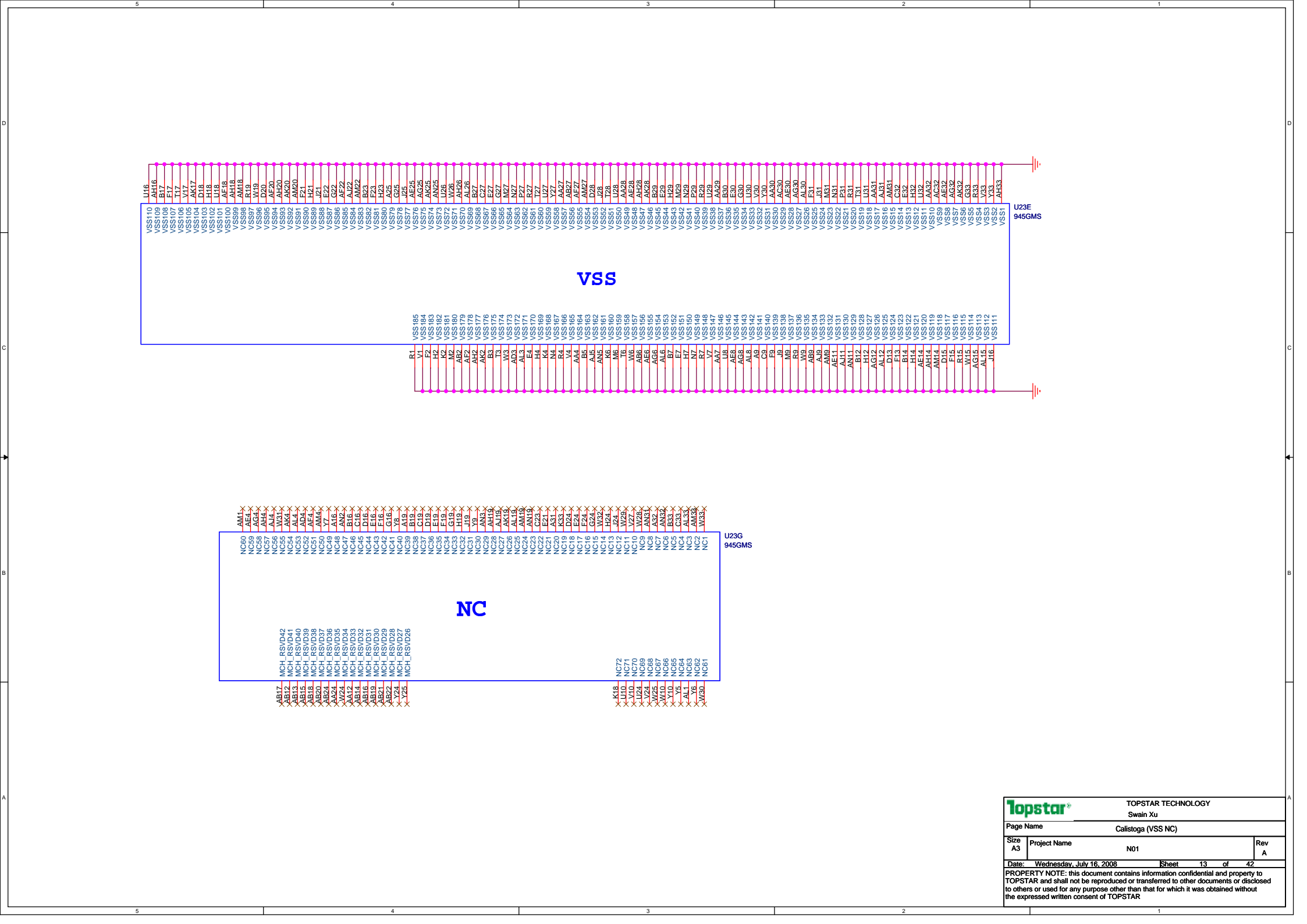


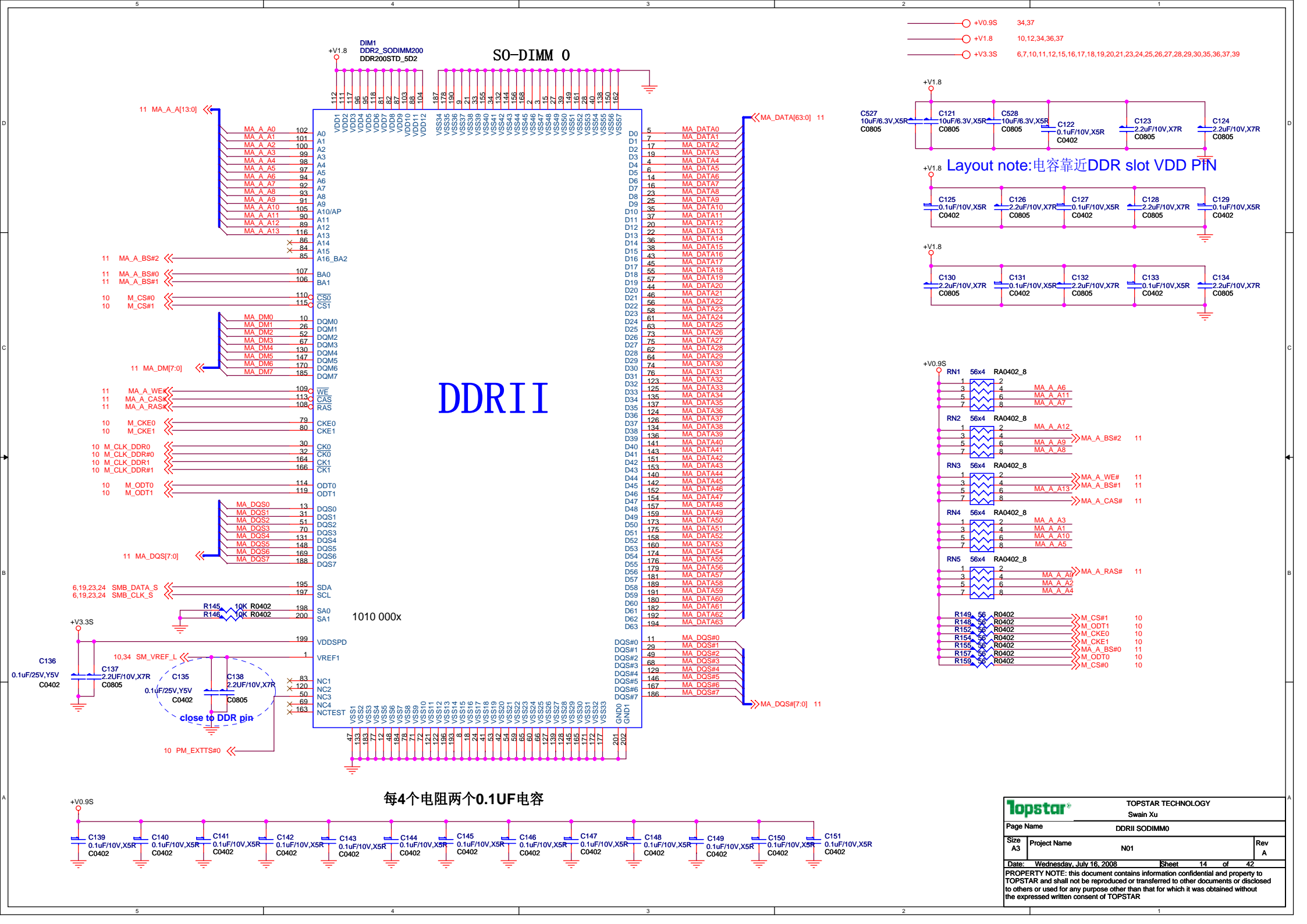


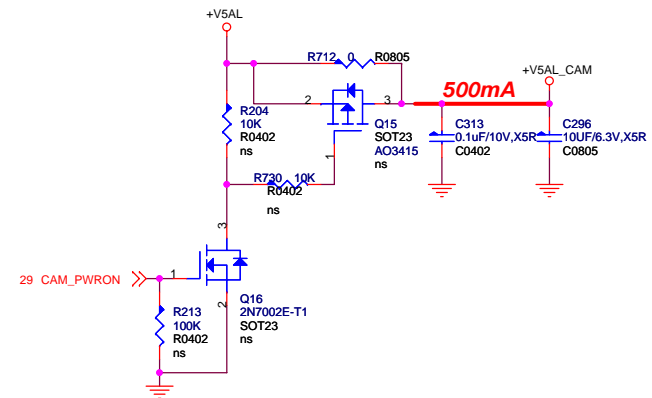
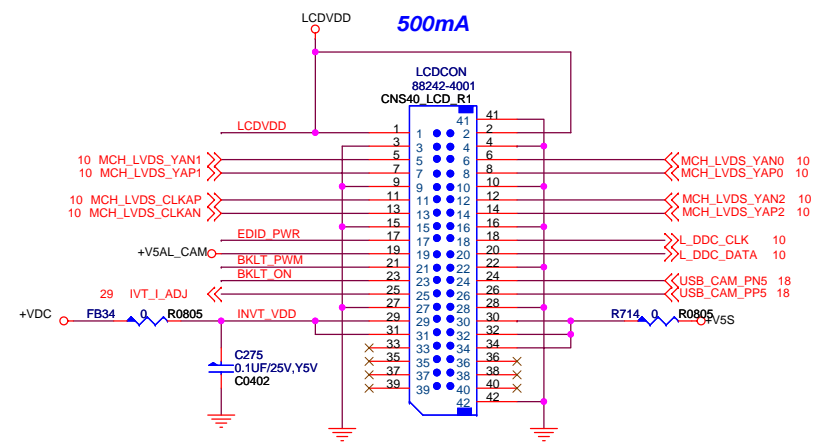
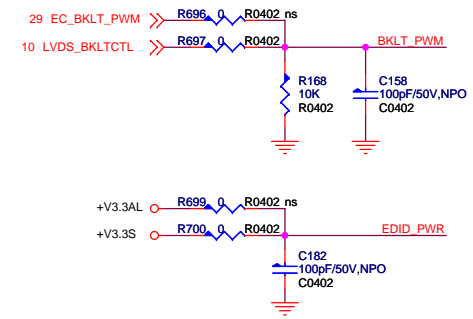
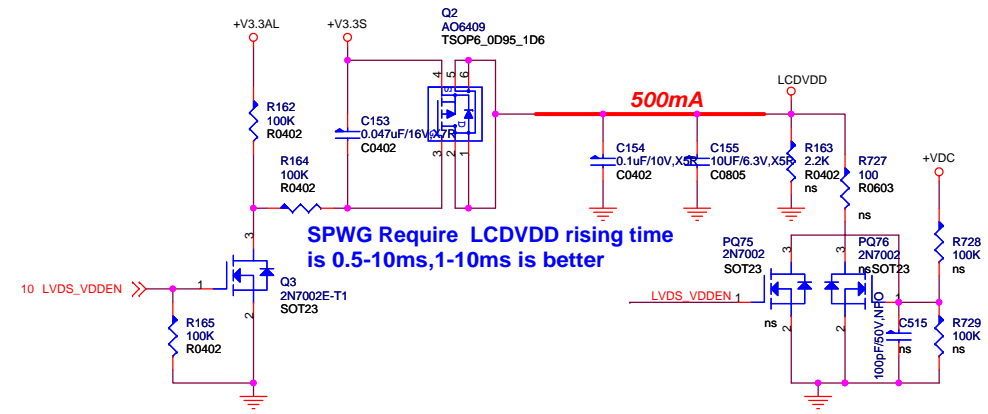
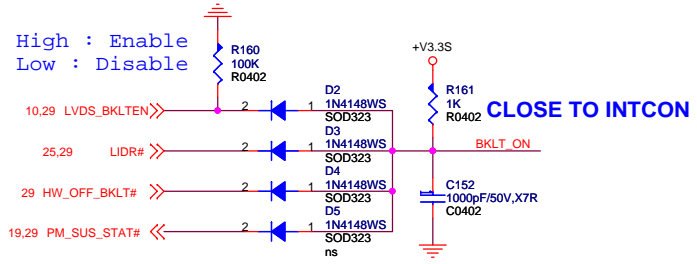




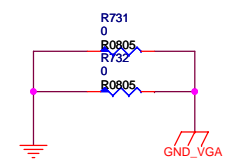
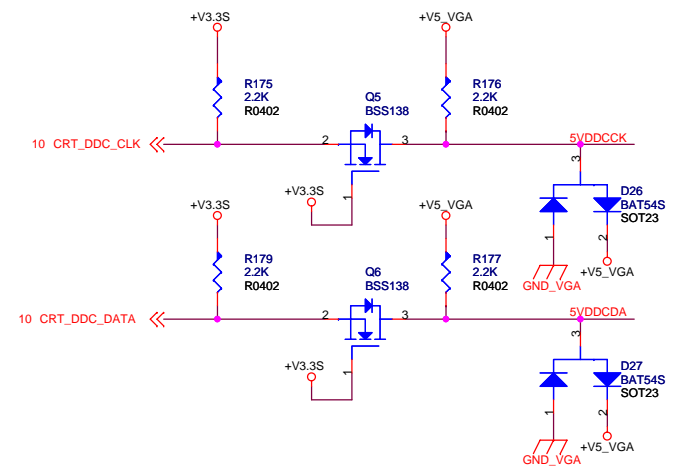
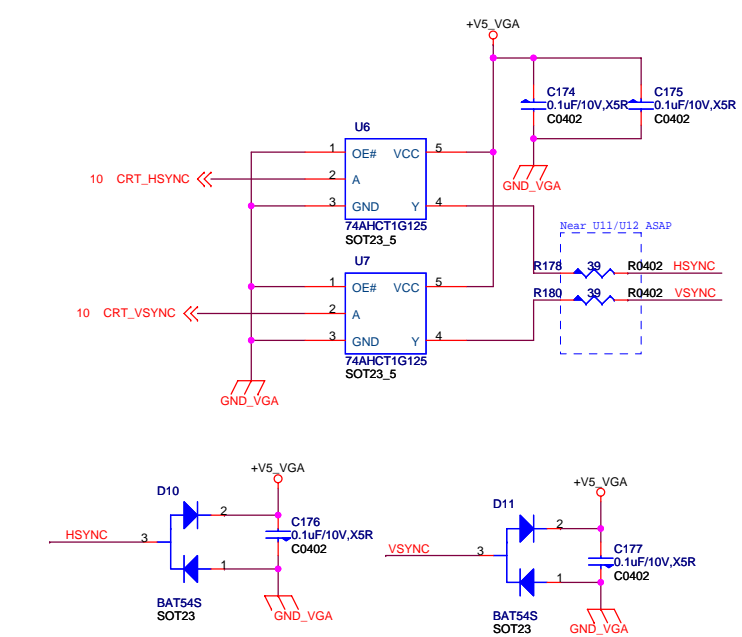
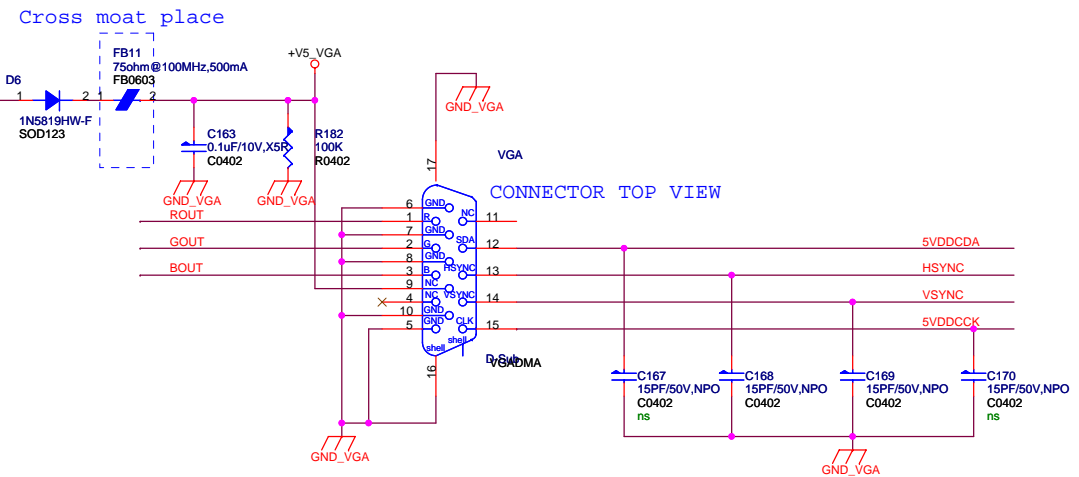
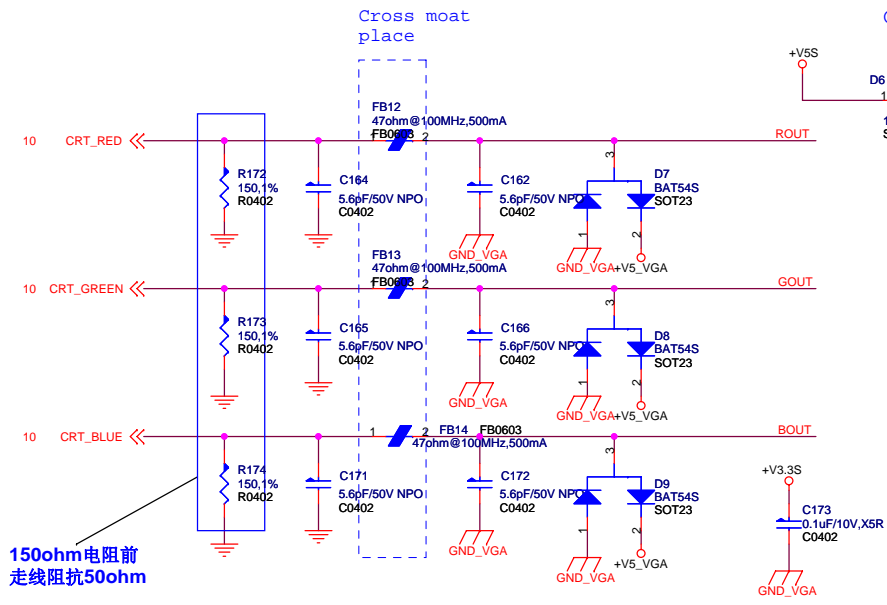


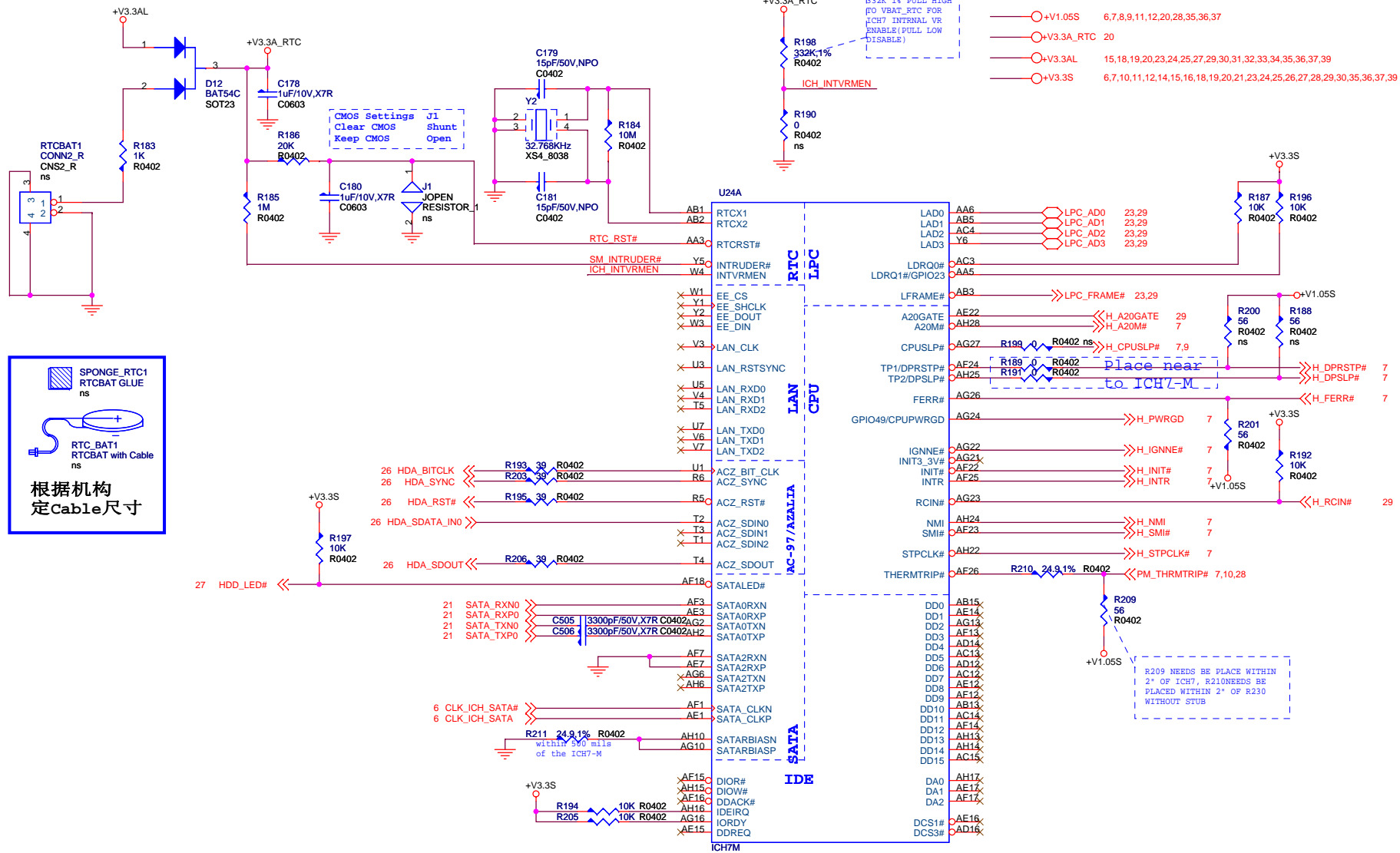


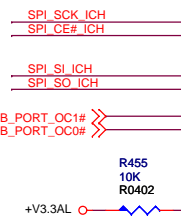
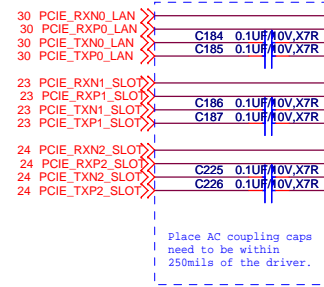
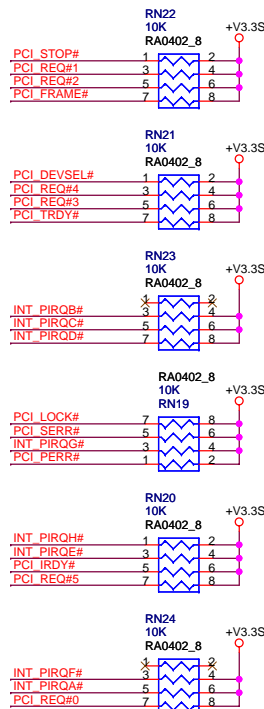
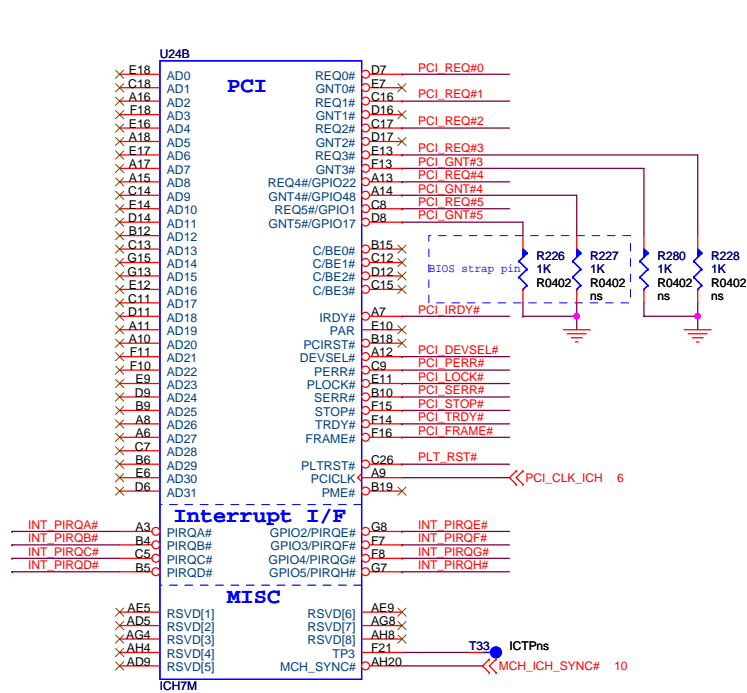




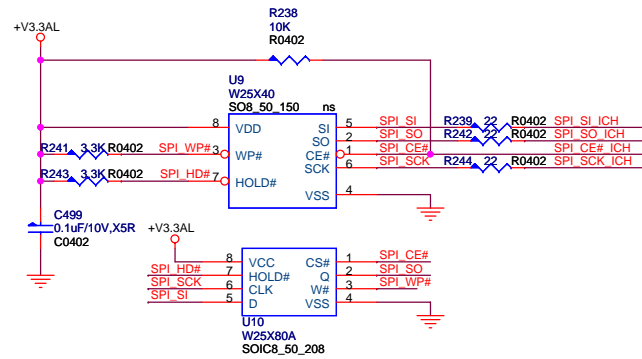
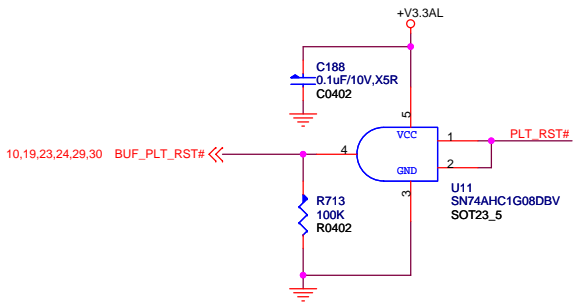
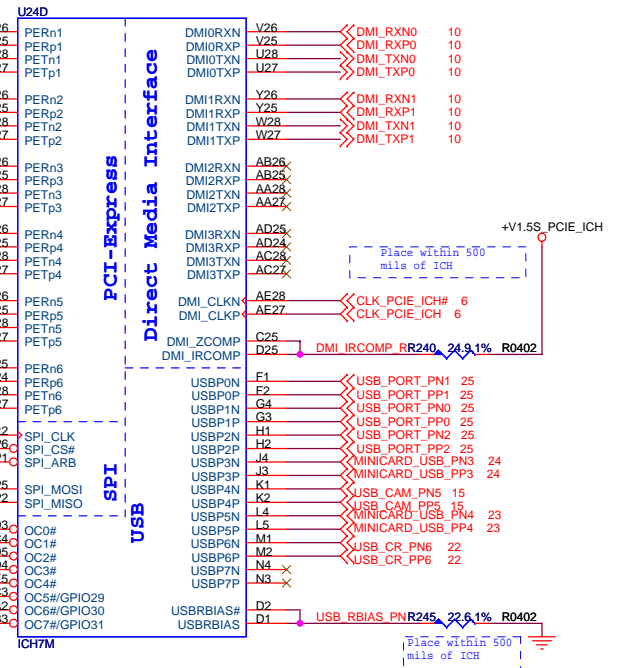
- +V3.3AL 17,18,19,20,23,24,25,27,29,30,31,32,33,34,35,36,37,39
- +V3.3S 6,7,10,11,12,14,16,17,18,19,20,21,23,24,25,26,27,28,29,30,35,36,37,39
- +V5AL 20,22,25,33,34,36,37
- +VDC 23,25,31,33,34,35,37,39
- +V5S 16,19,20,21,25,26,27,29,35,37,38,39



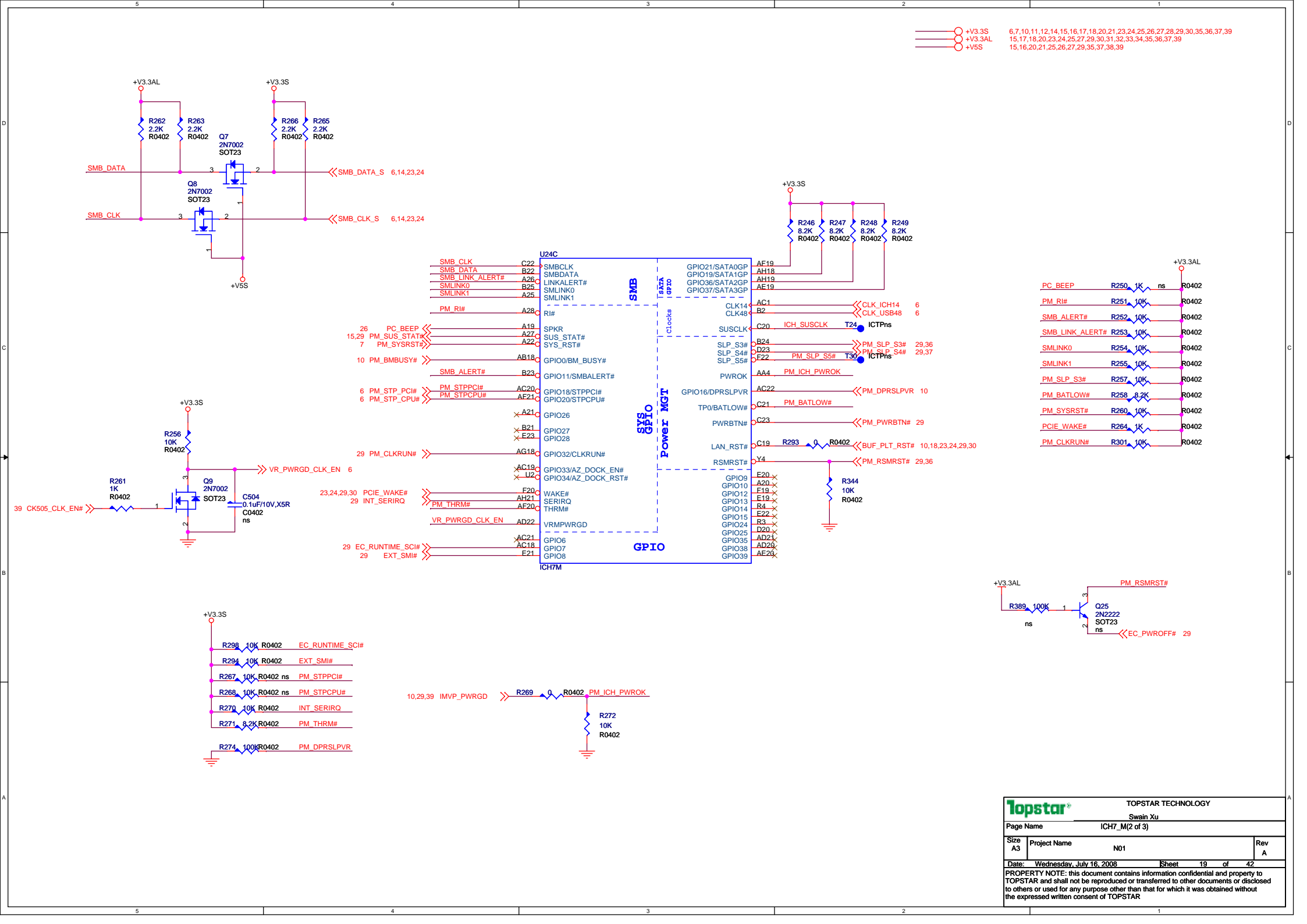


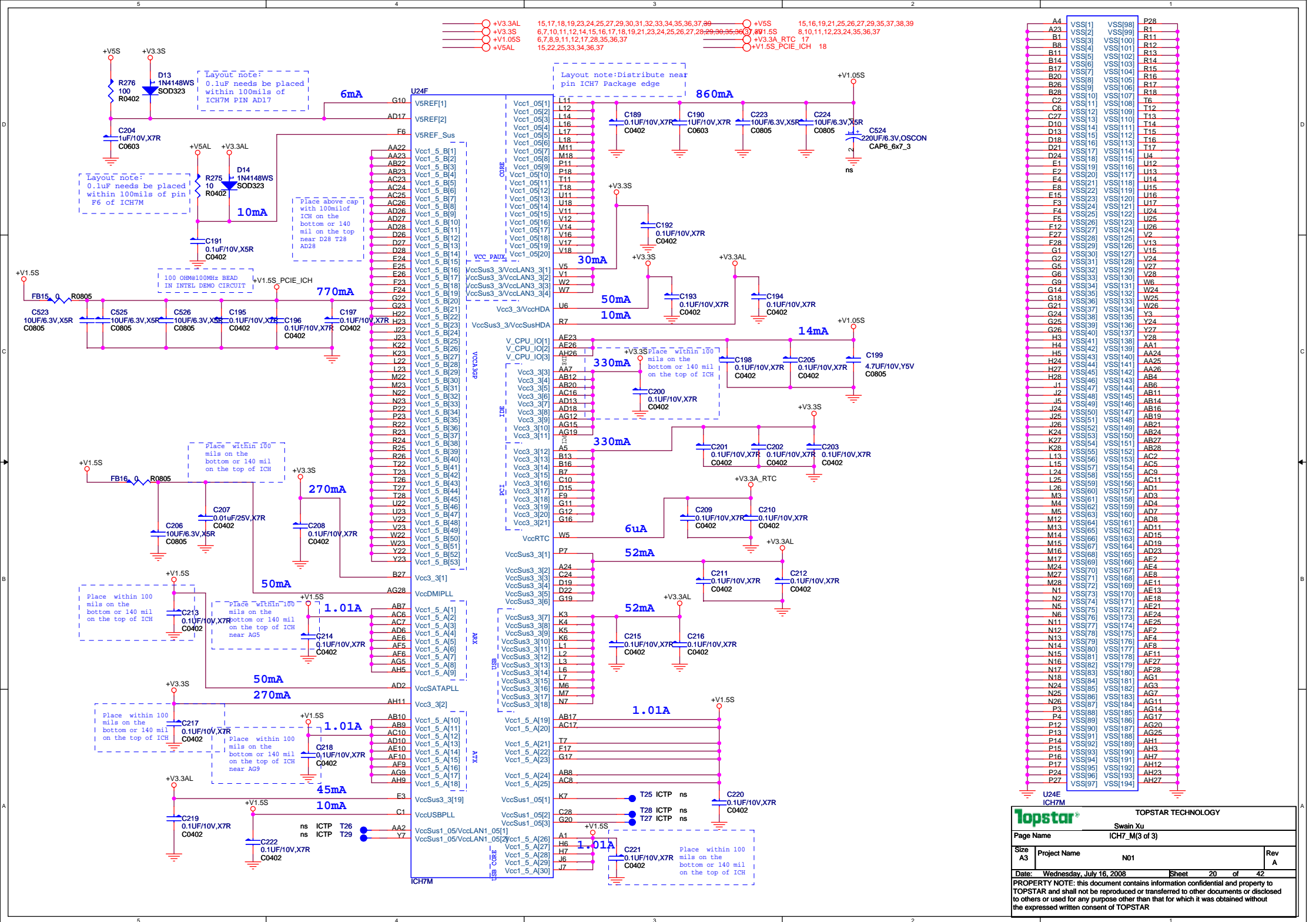


- +V1.5S_PCIE_ICH 20
- +V3.3S 6,7,10,11,12,14,15,16,17,19,20,21,23,24,25,26,27,28,29,30,35,36,37,39
- +V3.3AL 15,17,19,20,23,24,25,27,29,30,31,32,33,34,35,36,37,39

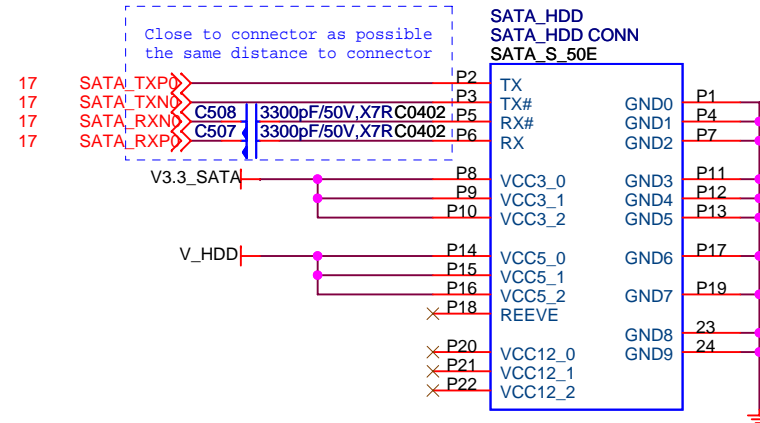
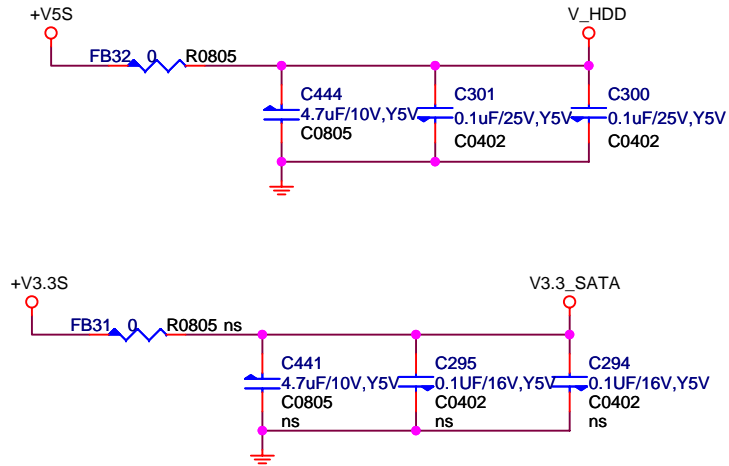


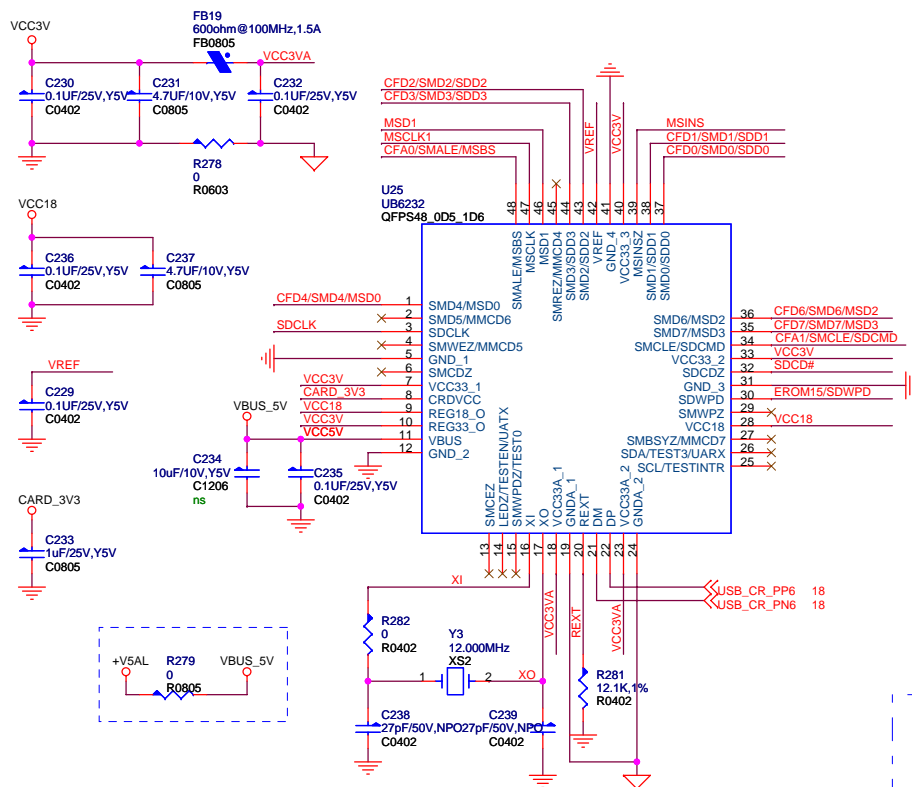
GNT5#	GNT4#	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC



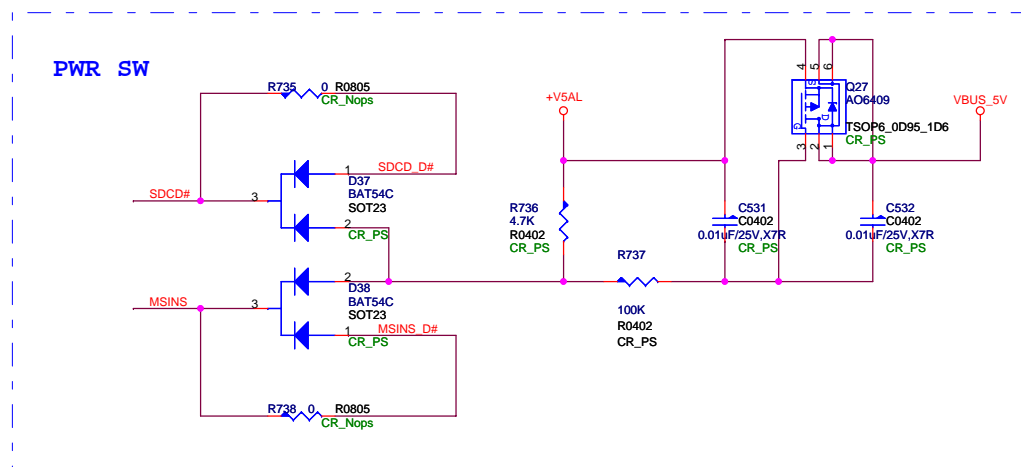
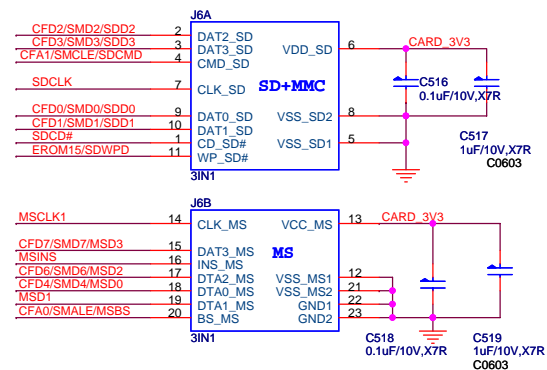


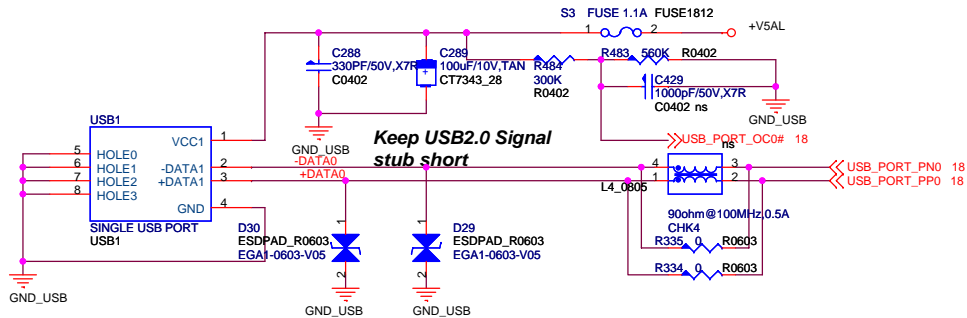
SATA HDD



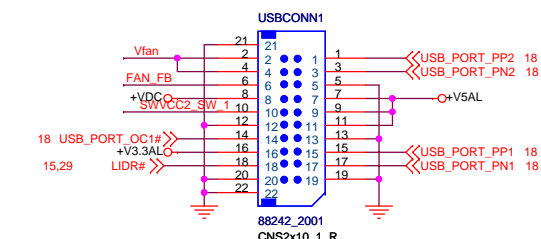
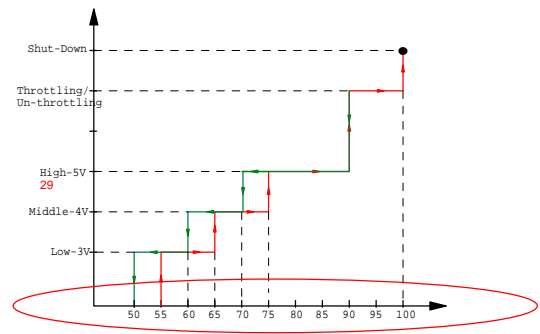
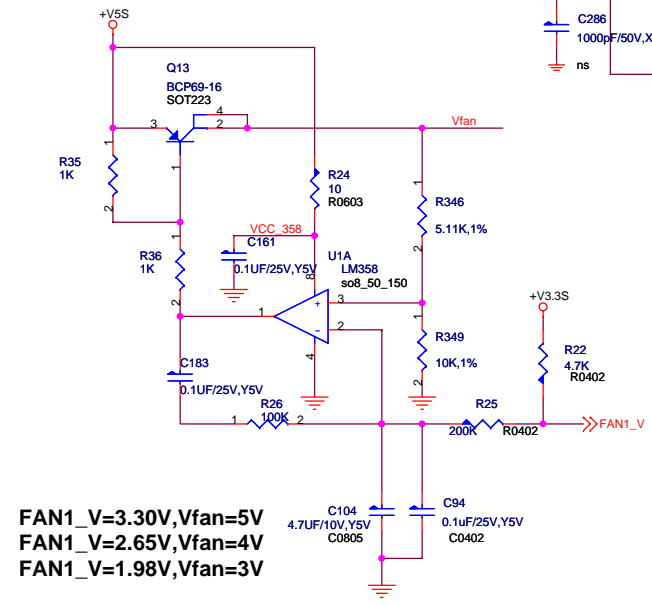
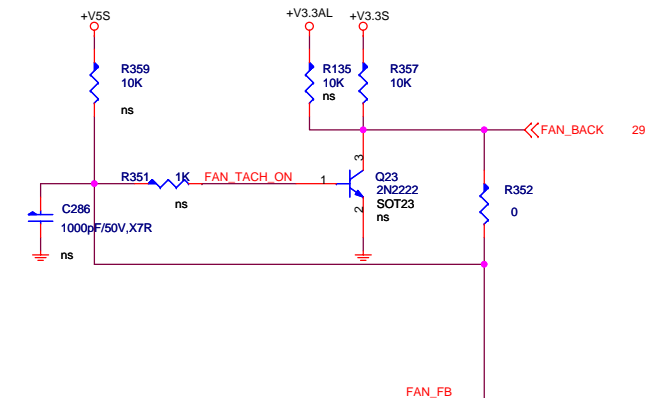
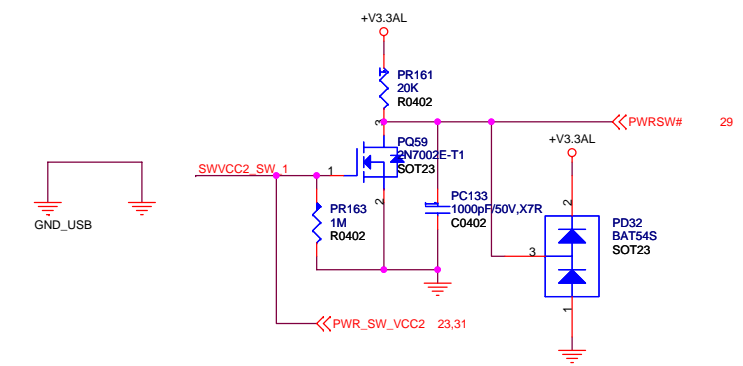


OLD 3IN1 CONN.



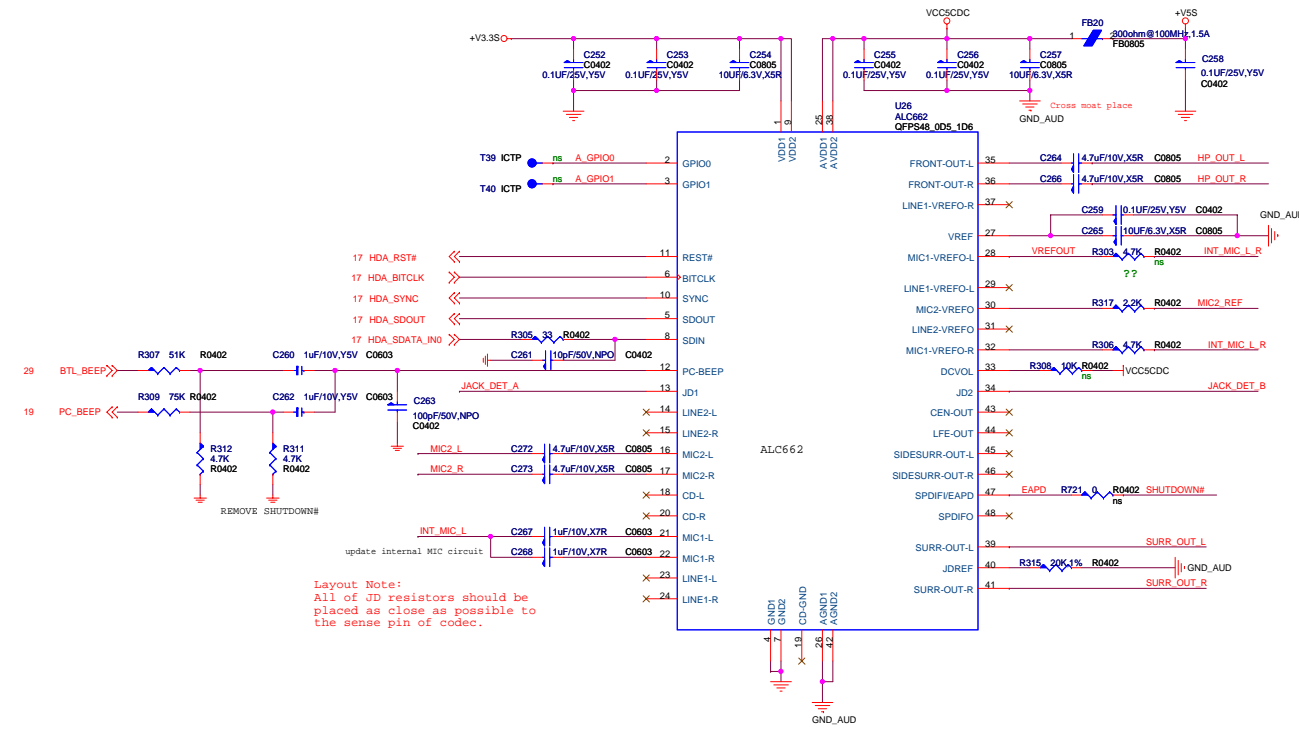


- +V3.3S 6,7,10,11,12,14,15,16,17,18,19,20,21,23,24,26,27,28,29,30,35,36,37,39
- +V3.3AL 15,17,18,19,20,23,24,27,29,30,31,32,33,34,35,36,37,39
- +V5S 15,16,19,20,21,26,27,29,35,37,38,39
- +V5AL 15,20,22,33,34,36,37
- +VDC 15,23,31,33,34,35,37,39



FAN1_V=3.30V,Vfan=5V
FAN1_V=2.65V,Vfan=4V
FAN1_V=1.98V,Vfan=3V

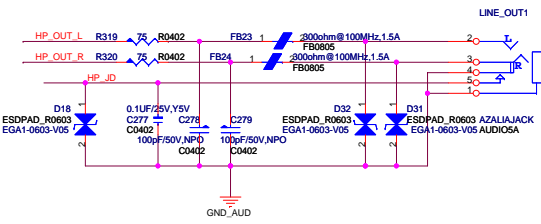
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+V3.3S
+V5S
6,7,10,11,12,14,15,16,17,18,19,20,21,23,24,25,27,28,29,30,35,36,37,39
15,16,19,20,21,25,27,28,35,37,38,39

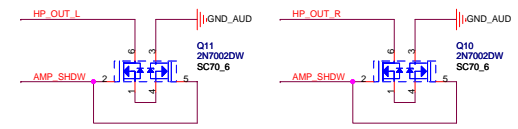
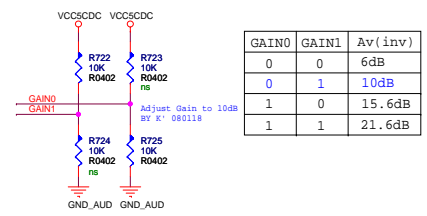
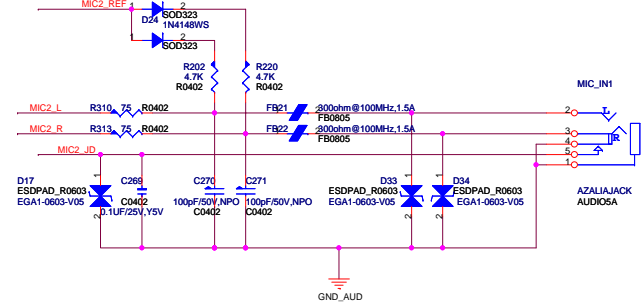
Headphone Jack

INPUT: HEADPHONE / LINE-OUT
OUTPUT: FRONT L/R

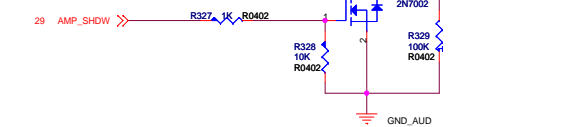


Stereo Microphone Jack

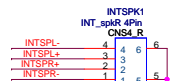
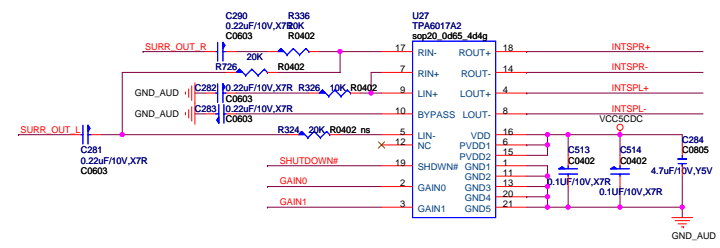
INPUT: STEREO MIC-IN
OUTPUT: CENT / LFE



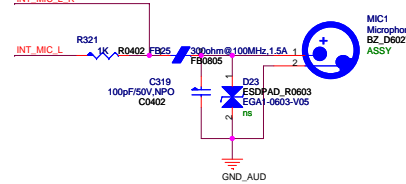
De-pop Solution



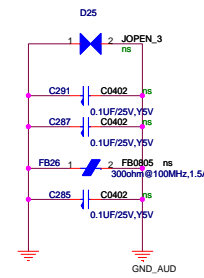
Onboard Amp



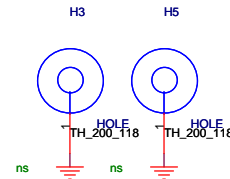
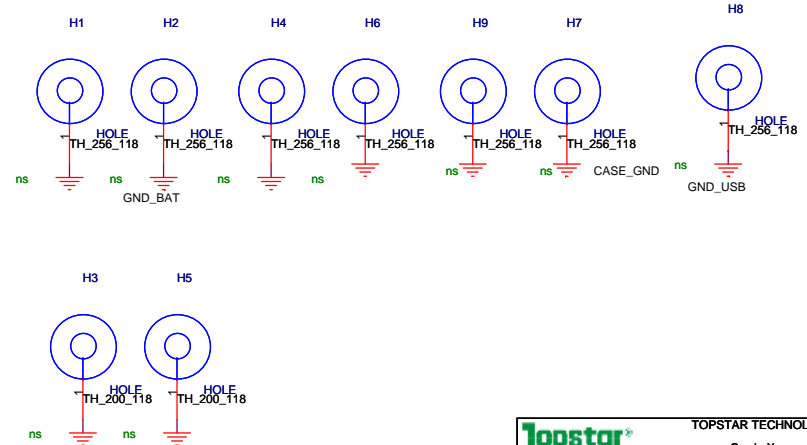
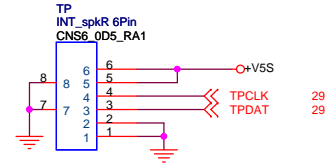
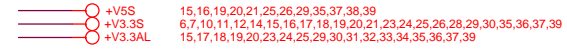
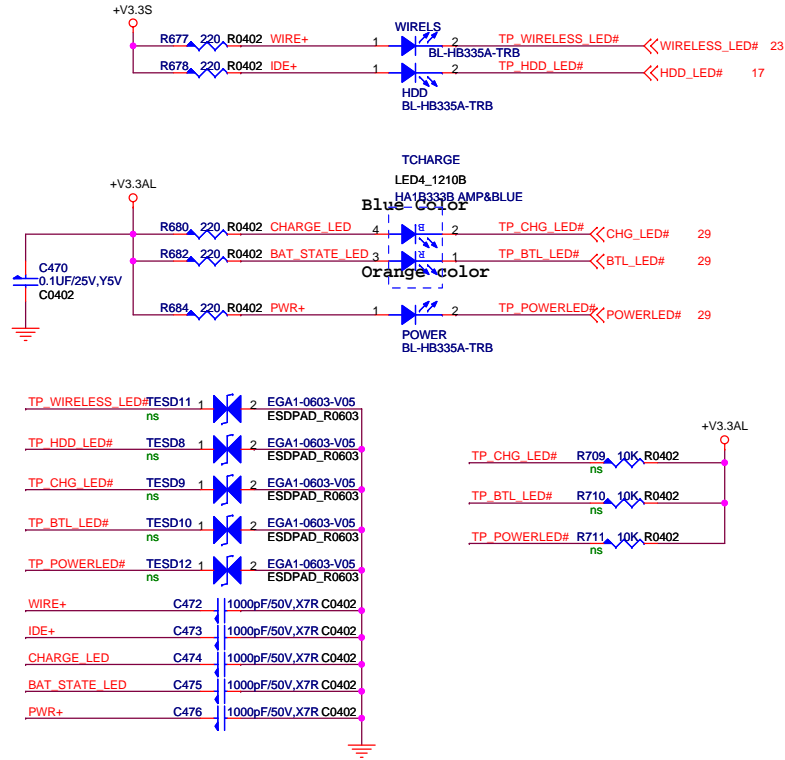
onboard stereo microphone



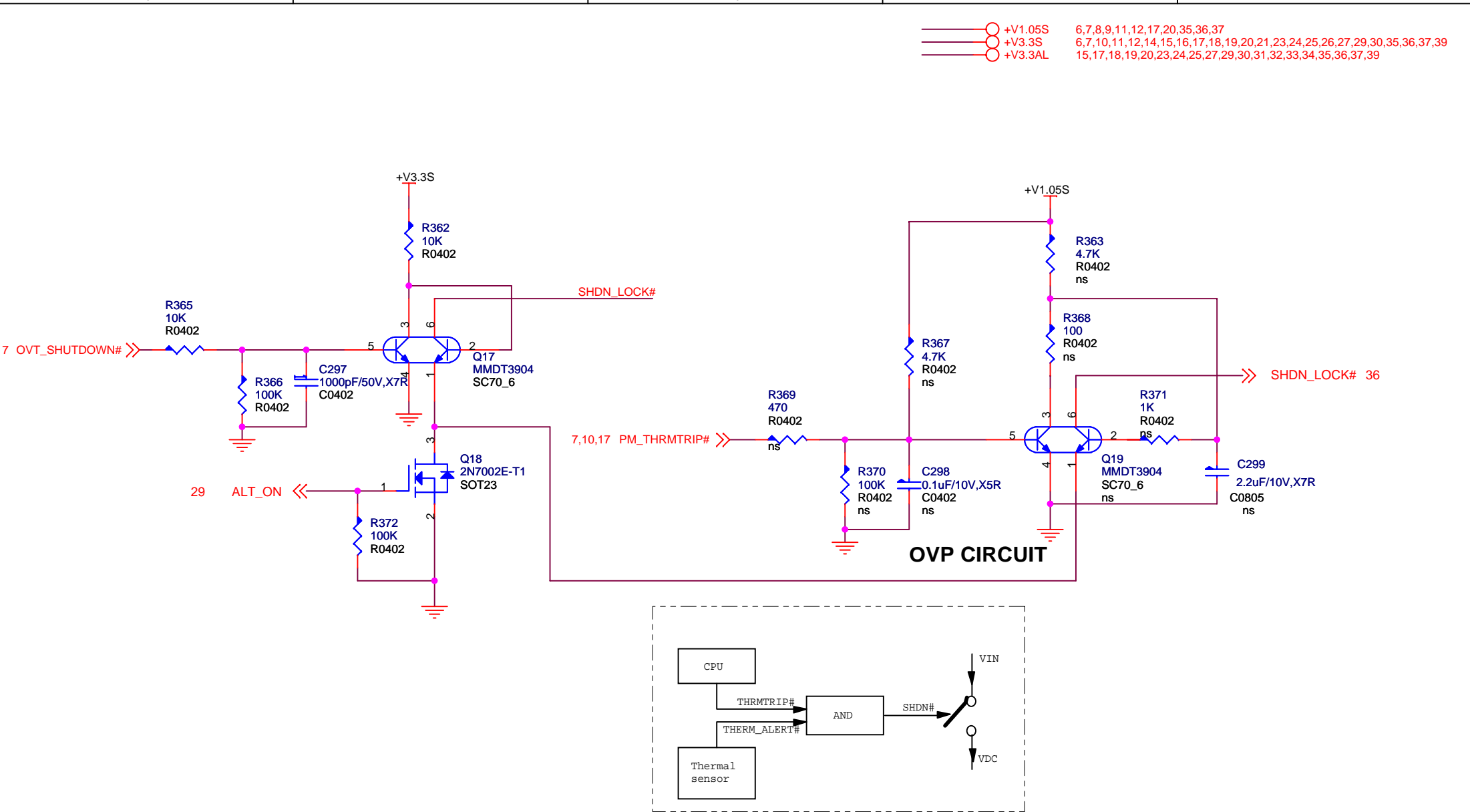
Layout Note:
Tied at three points under the codec and near the codec

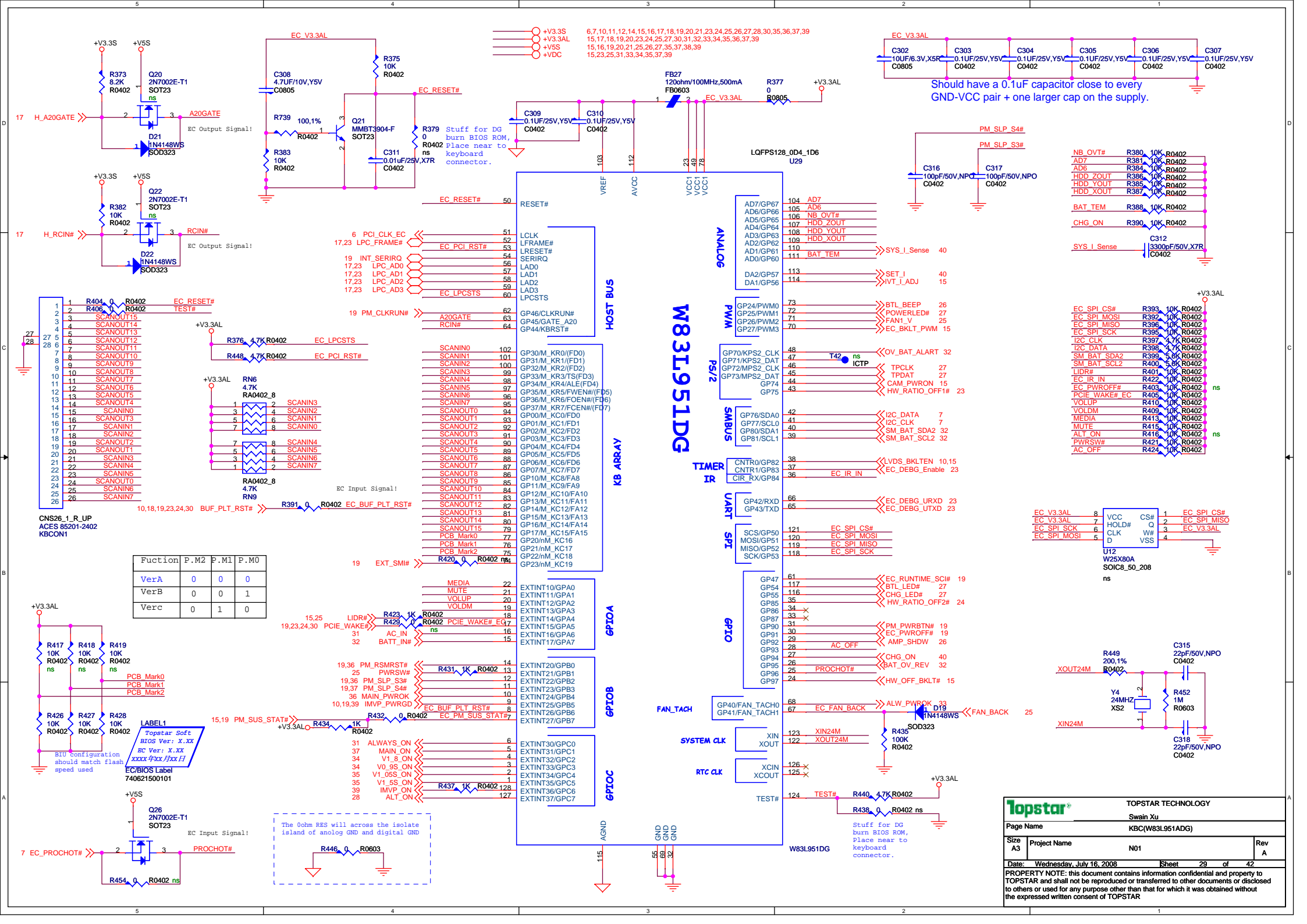


LED

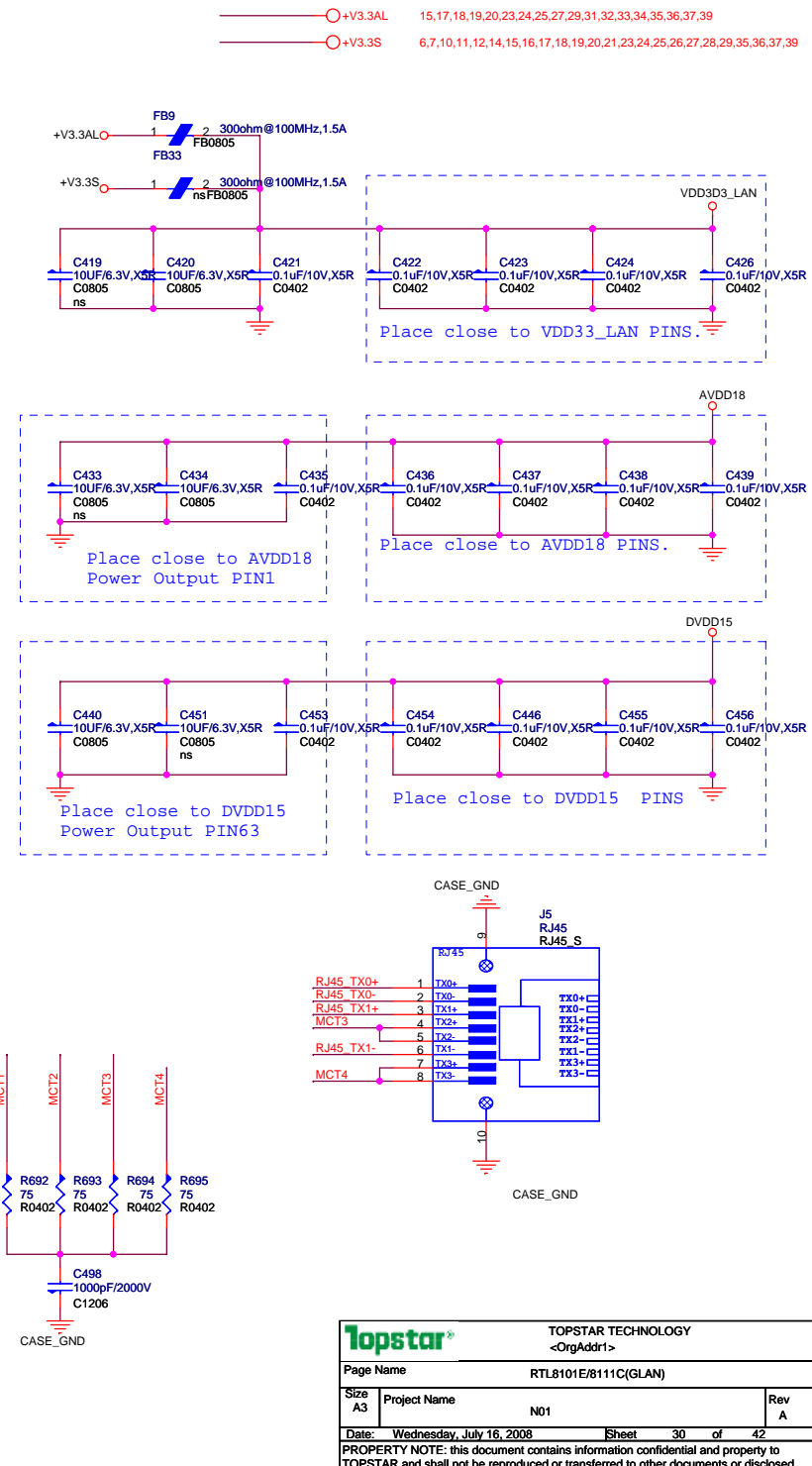


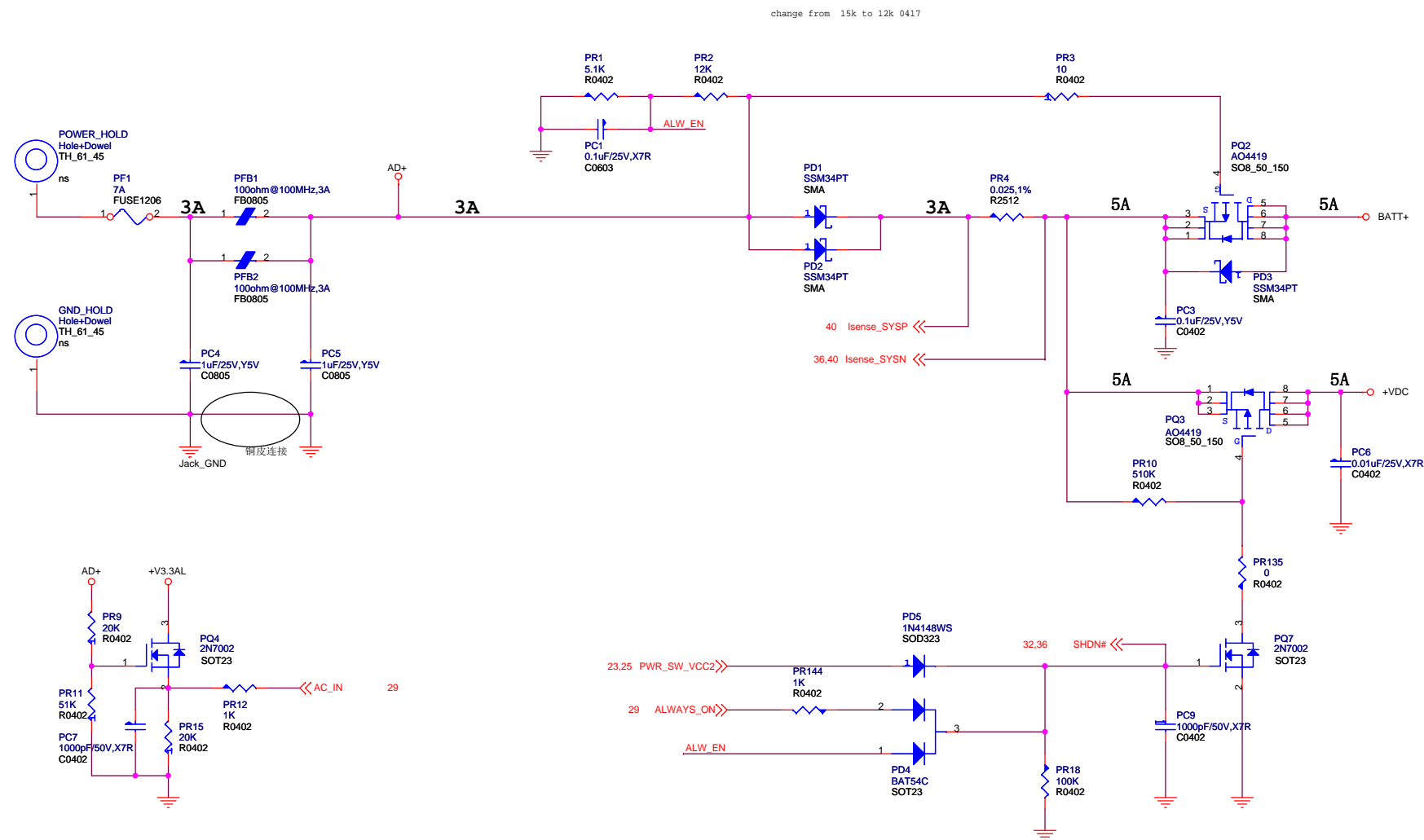
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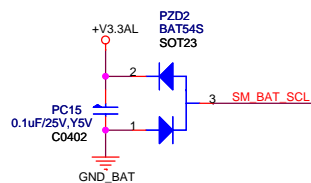
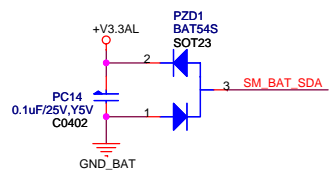
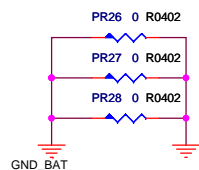
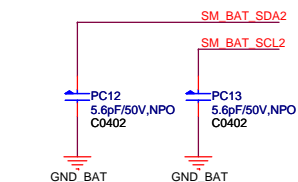
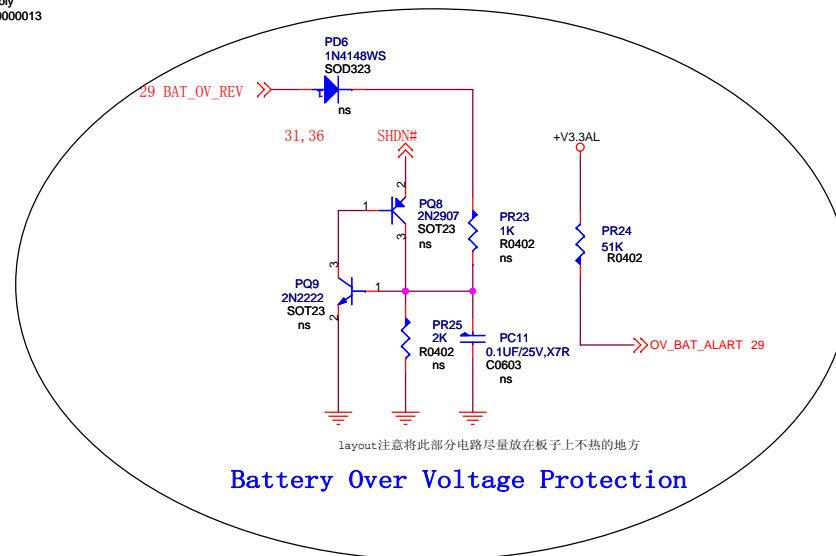
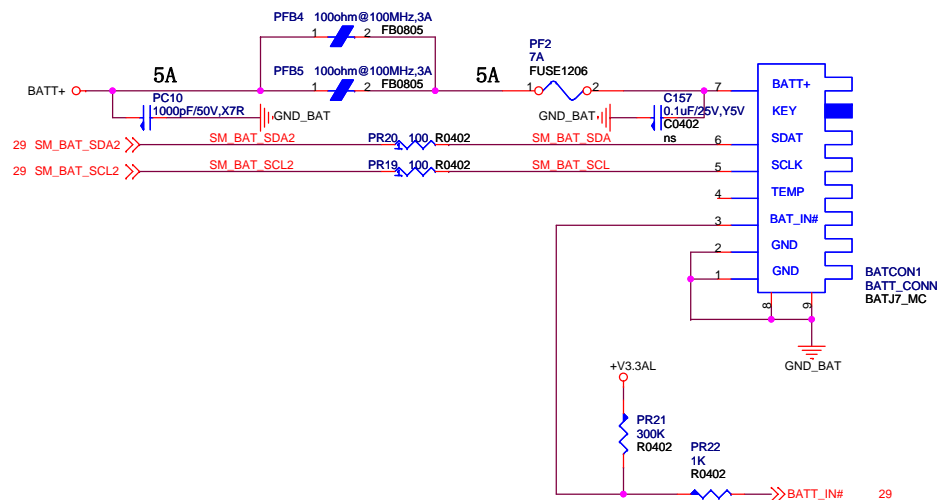




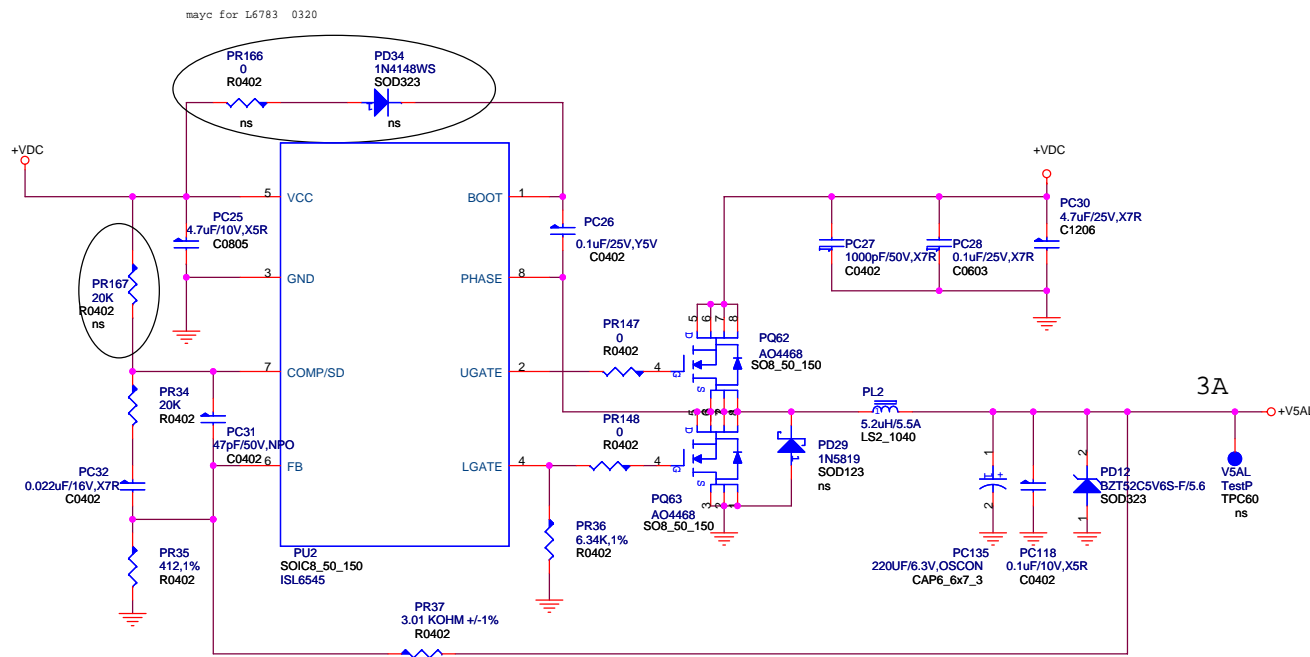
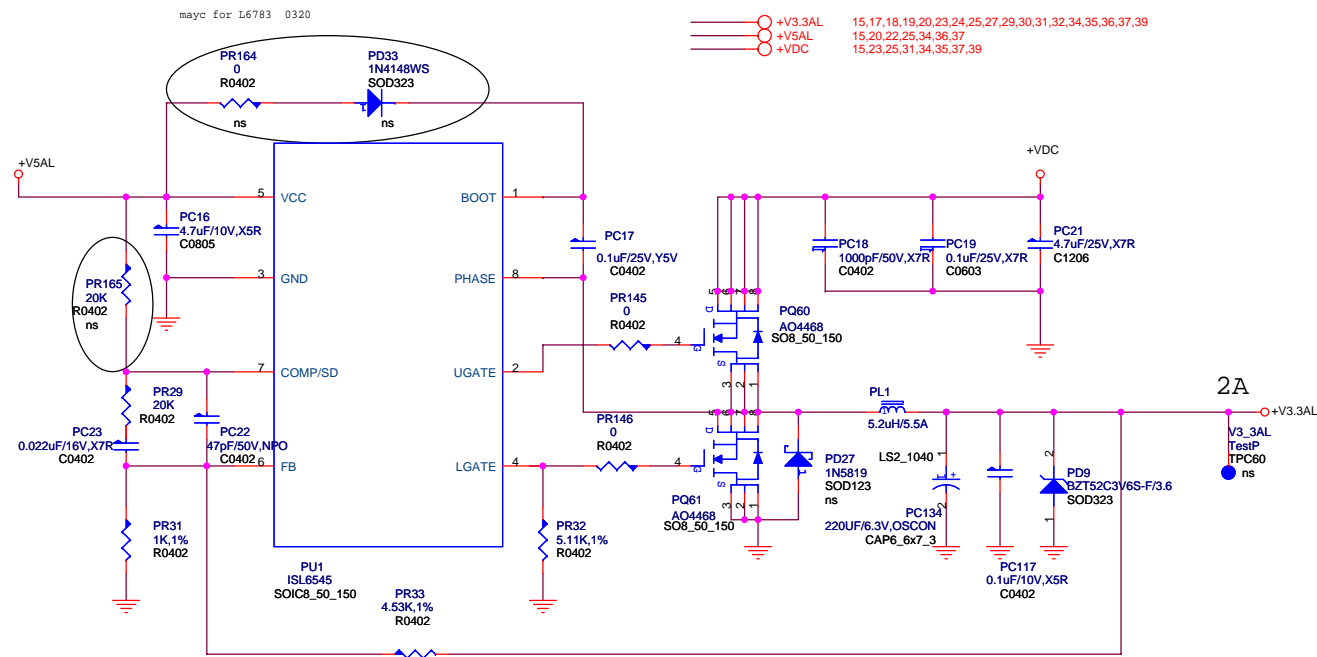
	RTL8101E
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AVDD18	1.8V
EVDD18	1.8V
DVDD15	1.5V

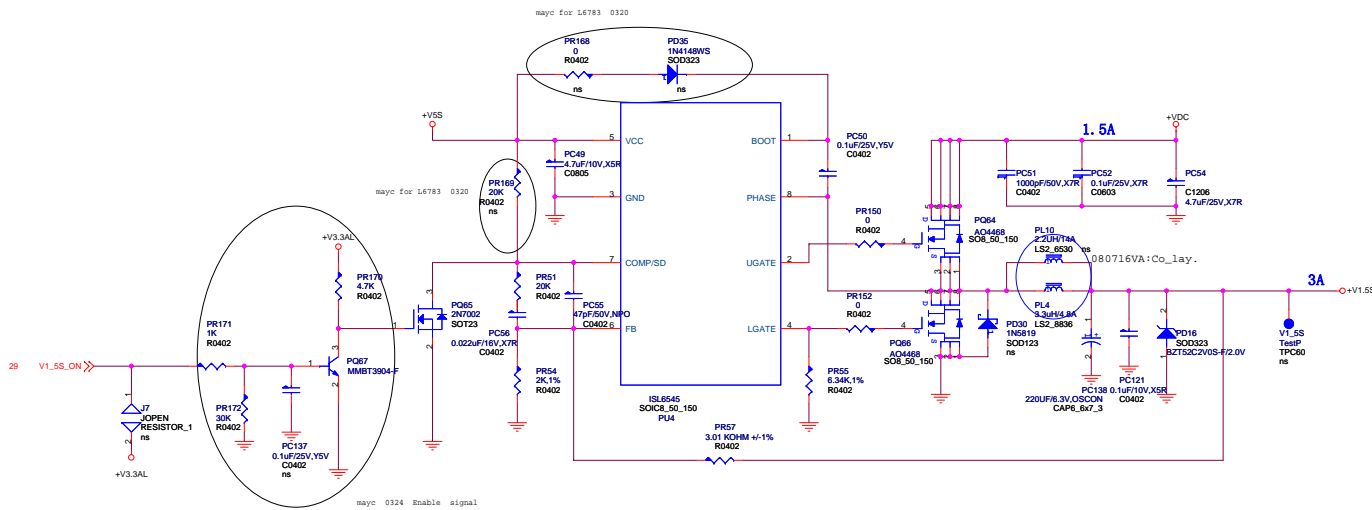




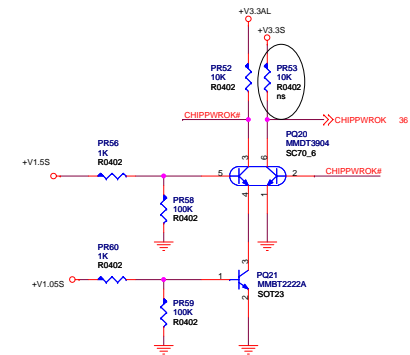
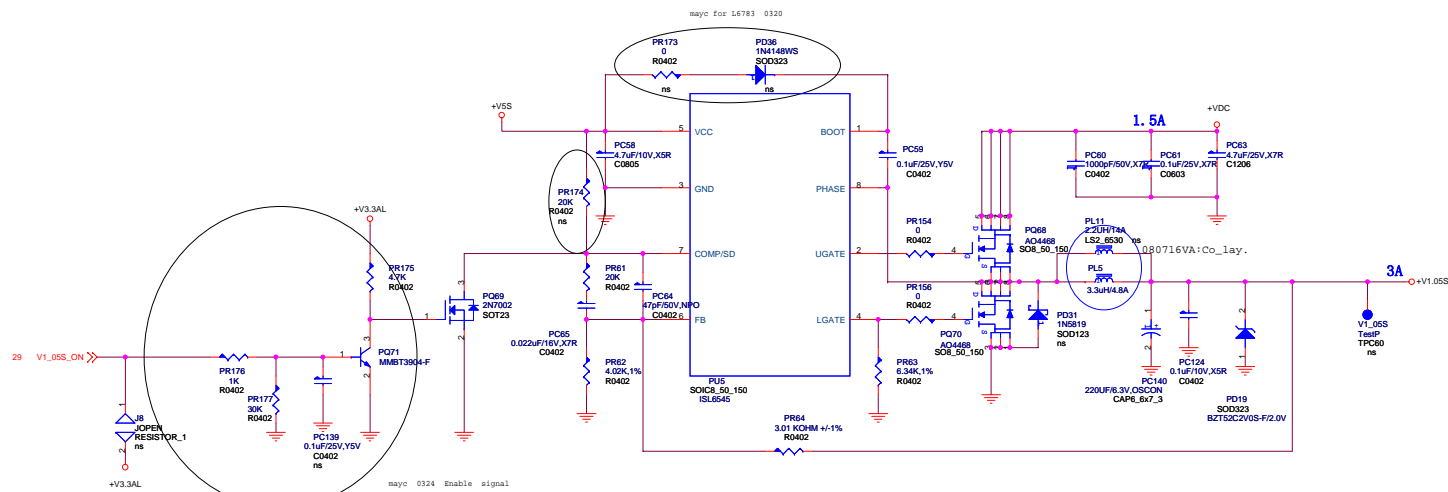


BATT+ 31,40
+V3.3AL 15,17,18,19,20,23,24,25,27,29,30,31,33,34,35,36,37,39

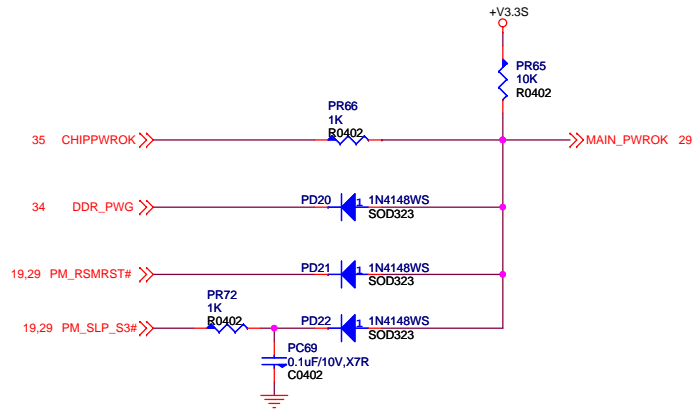




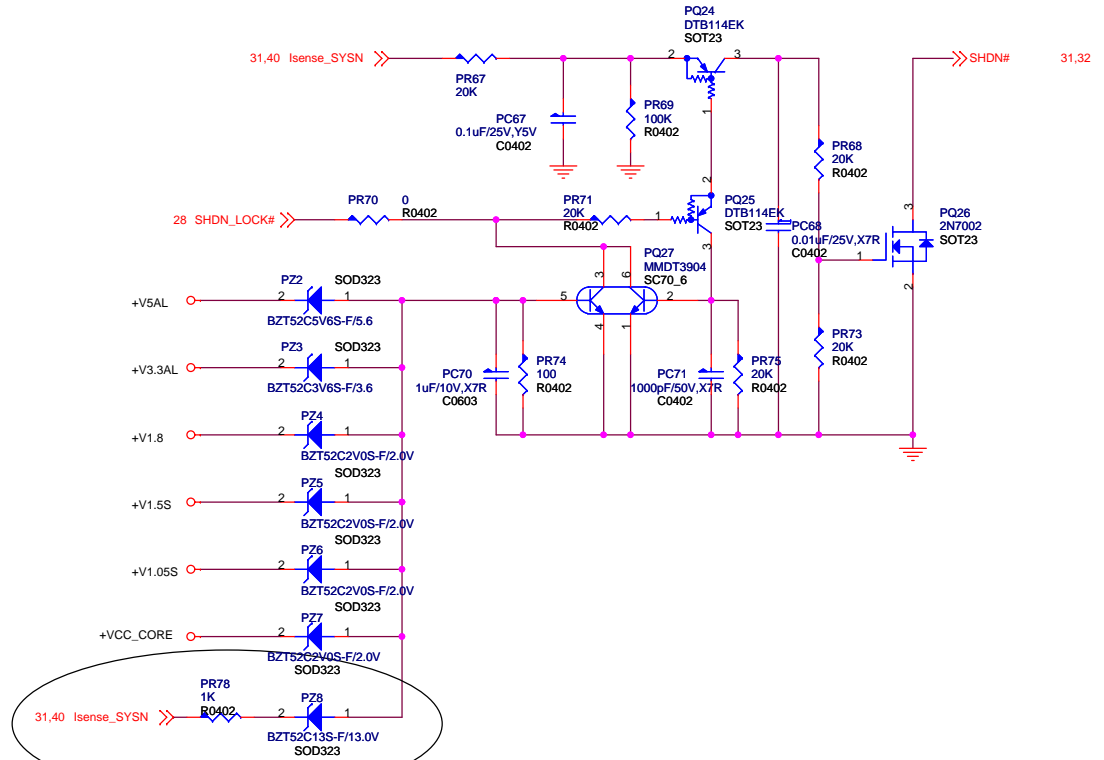
- +V3.3AL 15,17,18,19,20,23,24,25,27,29,30,31,32,33,34,36,37,39
- +V3.3S 6,7,10,11,12,14,15,16,17,18,19,20,21,23,24,25,26,27,28,29,30,36,37,39
- +VDC 15,23,25,31,33,34,37,39
- +V1.5S 8,10,11,12,20,23,24,36,37
- +V1.05S 6,7,8,9,11,12,17,20,28,36,37
- +VSS 15,16,19,20,21,25,26,27,29,37,38,39



Power Good Logic CIRCUIT



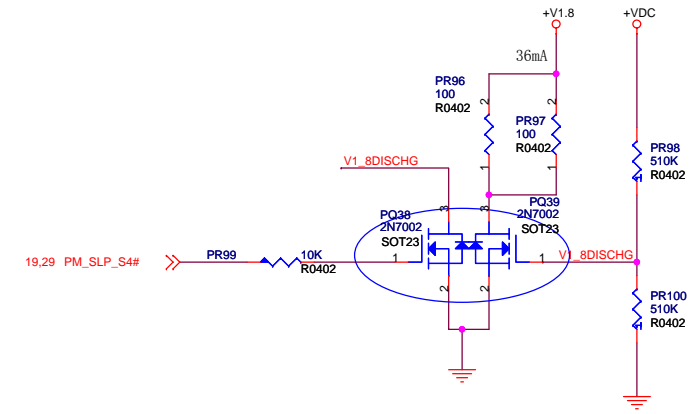
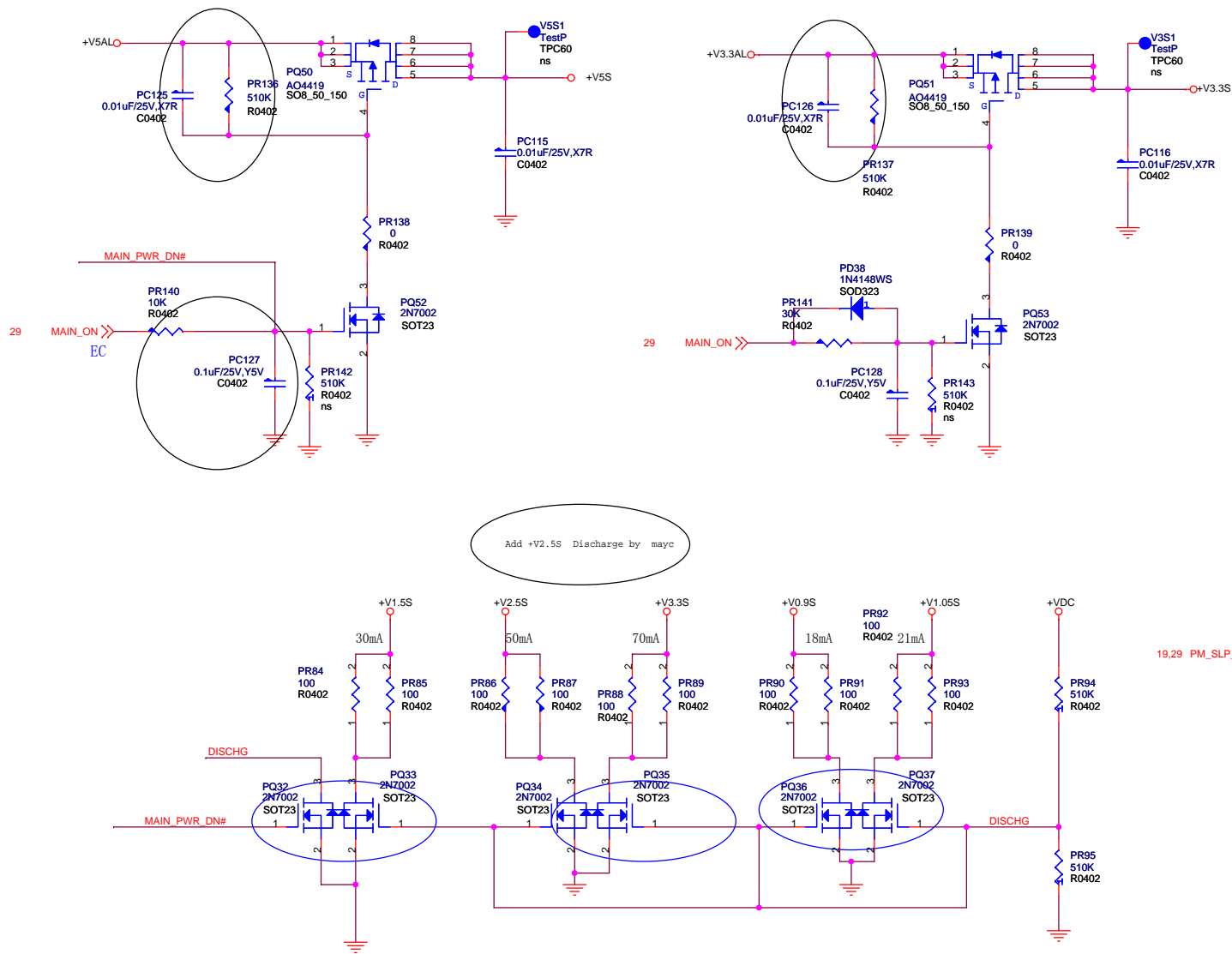
OVP CIRCUIT



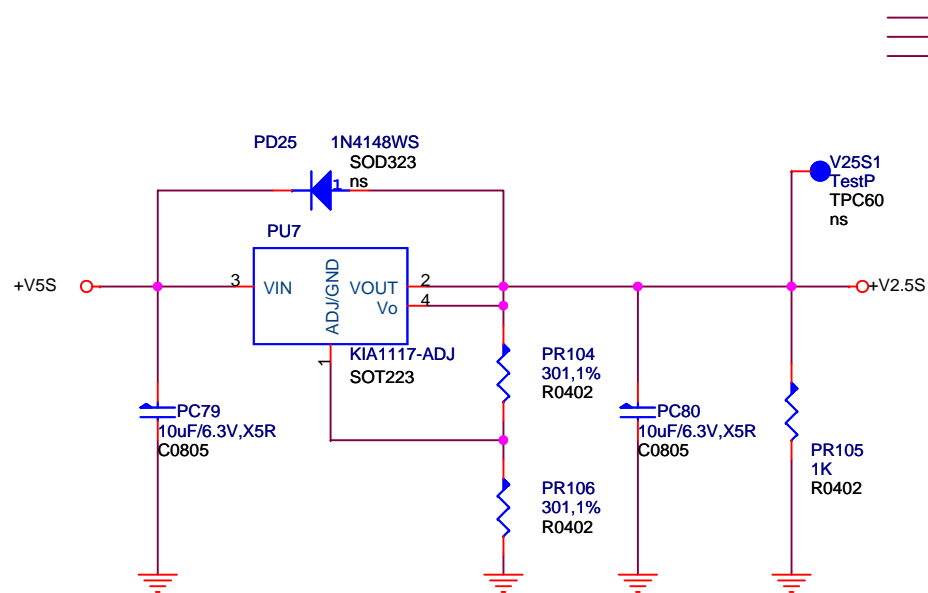
080716VA:新料,料号申请中.

+V3.3S	6,7,10,11,12,14,15,16,17,18,19,20,21,23,24,25,26,27,28,29,30,35,37,39
+V5AL	15,20,22,25,33,34,37
+V3.3AL	15,17,18,19,20,23,24,25,27,29,30,31,32,33,34,35,37,39
+V1.05S	6,7,8,9,11,12,17,20,28,35,37
+V1.5S	8,10,11,12,20,23,24,35,37
+VCC_CORE	8,39
+V1.8	10,12,14,34,37
+VDC	15,23,25,31,33,34,35,37,39

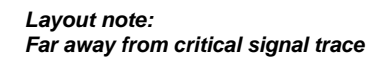
TOPSTAR TECHNOLOGY		Mayc
Page Name		Power Good Logic/OVP
Size A3	Project Name	N01
Date: Wednesday, July 16, 2008	Sheet	36 of 42
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- +V3.3S 6,7,10,11,12,14,15,16,17,18,19,20,21,23,24,25,26,27,28,29,30,35,36,39
- +V3.3AL 15,17,18,19,20,23,24,25,27,29,30,31,32,33,34,35,36,39
- +V5S 15,16,19,20,21,25,26,27,29,35,38,39
- +V5AL 15,20,22,25,33,34,36
- +V1.5S 8,10,11,12,20,23,24,35,36
- +V2.5S 12,38
- +V0.9S 14,34
- +V1.05S 6,7,8,9,11,12,17,20,28,35,36
- +VDC 15,23,25,31,33,34,35,39
- +V1.8 10,12,14,34,36

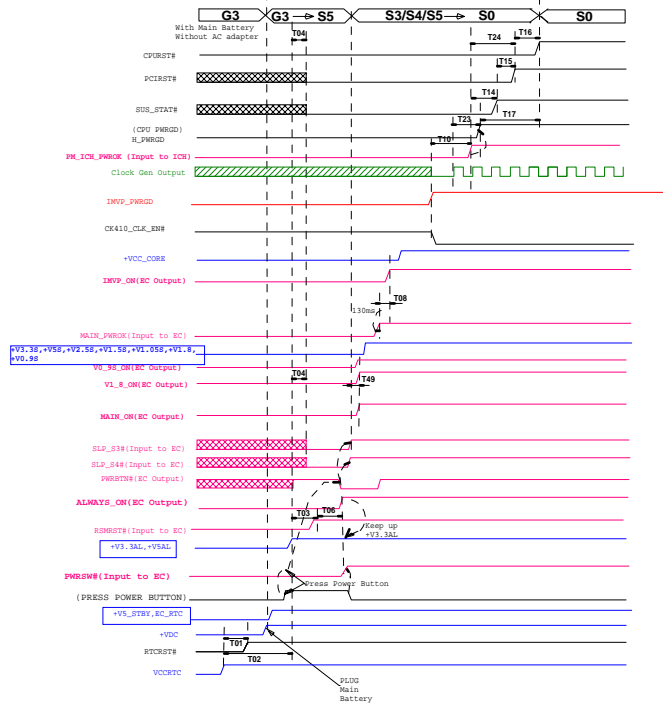


+V3.3AL 15,17,18,19,20,23,24,25,27,29,30,31,32,33,34,35,36,37,39
+V2.5S 12,37
+V5S 15,16,19,20,21,25,26,27,29,35,37,39

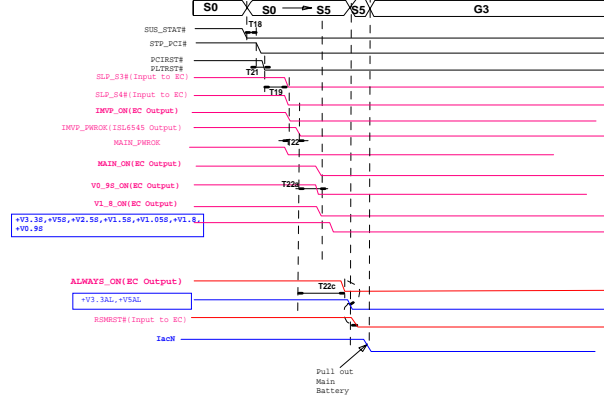


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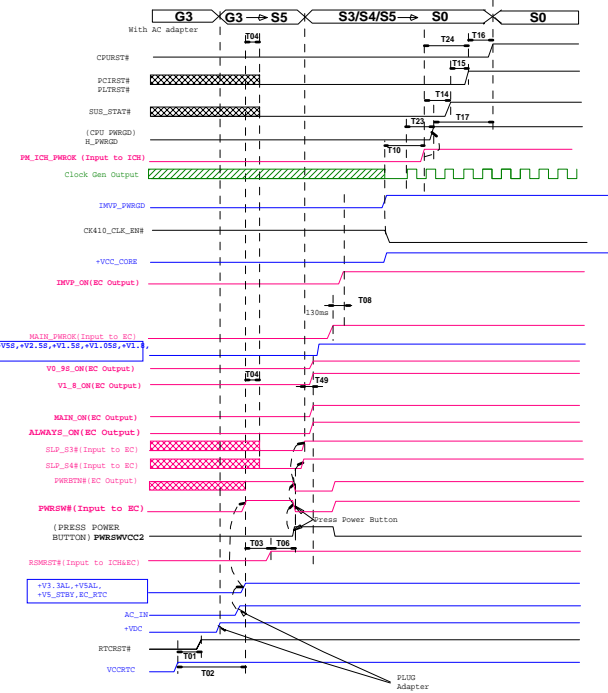
Power On Sequence(Battery mode)



Power Off Sequence(Battery Mode)



Power On Sequence(Adapter mode)



Power Off Sequence(Adapter Mode)

